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(54) Semiconductor memory device and method of manufacturing the same

(57) A semiconductor memory device having MIS transistors to constitute memory cells (MC), each of the MIS transistors comprising a semiconductor layer (12), a source region (15) formed in the semiconductor layer, a drain region (14) formed apart from the source region in the semiconductor layer, the semiconductor layer between the source region and the drain region serving as a channel body in a floating state, a main gate (13) provided between the source region and the drain region to form a channel in the channel body; and an auxiliary gate (20) provided separately from the main gate to control a potential of the channel body by capacitive coupling, the auxiliary gate being driven in synchronization with the main gate. The MIS transistor has a first date state in which the channel body is set at a first potential and a second data state in which the channel body is set at a second potential.

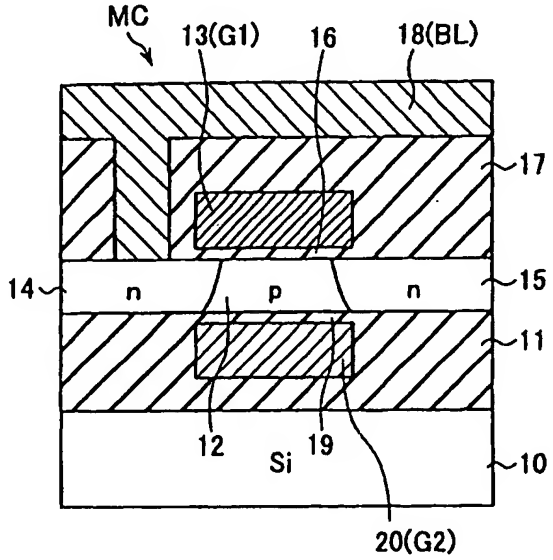

FIG. 3

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is more unfavorable than ordinary SRAM and DRAM.

[0010] Japanese Patent Laid-open No. Hei 8-213624 discloses a gain cell of a type configured to store charge with a channel body as a storage node and use the fact that there is difference in parasitic bipolar collector current depending on the potential of the channel body. Also in this gain cell, it is necessary to write "1" before writing "0", and regarding write speed, it is more unfavorable than ordinary SRAM and DRAM.

[0011] As described above, those recently proposed as a new DRAM need a special transistor structure and hence they have a complicated structure. Alternatively, even if they have a relatively simple structure, they have a drawback in controllability, whereby the achievement of high integration and high performance is difficult.

SUMMARY OF THE INVENTION

[0012] In order to accomplish the aforementioned and other objects, according to one aspect of the present invention, a semiconductor memory device having MIS transistors to constitute memory cells, each of the MIS transistors comprising:

a semiconductor layer;
a source region formed in the semiconductor layer;
a drain region formed apart from the source region in the semiconductor layer, the semiconductor layer between the source region and the drain region serving as a channel body in a floating state;
a main gate provided between the source region and the drain region to form a channel in the channel body; and
an auxiliary gate provided separately from the main gate to control a potential of the channel body by capacitive coupling, the auxiliary gate being driven in synchronization with the main gate,

wherein the MIS transistor has a first data state in which the channel body is set at a first potential and a second data state in which the channel body is set at a second potential.

[0013] According to another aspect of the present invention, a semiconductor memory device having MIS transistors to constitute memory cells, each of the MIS transistors having a first data state and a second data state, the semiconductor memory device, comprising:

a first semiconductor substrate;
auxiliary gates of the MIS transistors formed on the first semiconductor substrate to continue in one direction while their bottom faces and side faces are covered with an insulating film;
a second semiconductor substrate provided on the auxiliary gates with a first gate insulating film therebetween;
main gates of the MIS transistors formed on the second semiconductor substrate with a second gate insulating film to continue in parallel with the auxiliary gates;
source regions formed in space portions between the main gates and the auxiliary gates in the second semiconductor substrate;
drain regions formed apart from the source regions in space portions between the main gates and the auxiliary gates in the second semiconductor substrate;
source lines provided to be in contact with the source regions and continue in parallel with the main gates and the auxiliary gates;
an interlayer dielectric film covering the source lines; and
bit lines formed on the interlayer dielectric film in a direction intersecting the main gates and the auxiliary gates and being in contact with the drain regions.

[0014] According to a further aspect of the present invention, a method of manufacturing a semiconductor memory device, comprising:

forming an auxiliary gate on a first semiconductor substrate with a first gate insulating film therebetween;
forming an insulating film which is planarized after covering the auxiliary gate;
sticking a second semiconductor substrate on the insulating film;
polishing the first semiconductor substrate to form a semiconductor layer with a predetermined thickness;
forming a device isolation insulating film for device isolation in the first semiconductor substrate;
forming a main gate which faces the auxiliary gate on the semiconductor layer with the first gate insulating film therebetween; and
forming a source region and a drain region by ion-implanting impurities into the semiconductor layer with the main gate as a mask.

[0015] According to a still further aspect of the present invention, a method of manufacturing a semiconductor memory device, comprising:

forming a main gate on a first semiconductor substrate with a first gate insulating film therebetween;
forming a first insulating film which is planarized after covering the main gate;
sticking a second semiconductor substrate on the first insulating film;
polishing the first semiconductor substrate to form a semiconductor layer with a predetermined thickness;
forming a device isolation insulating film for device isolation in the first semiconductor substrate;
forming a second insulating film on the semiconduc-

DRAM cell used in respective embodiments;
Fig. 2 is a diagram showing the relation between body potential and gate bias for explaining the operational principle of the DRAM cell;
Fig. 3 is a diagram showing the sectional structure of a DRAM cell according to a first embodiment of the present invention;
Fig. 4 is a diagram showing an equivalent circuit of a cell array using the DRAM cells;
Fig. 5 is a diagram showing the layout of the cell array;
Fig. 6A is a sectional view taken along the line A-A' in Fig. 5;
Fig. 6B is a sectional view taken along the line B-B' in Fig. 5;
Fig. 7A is a waveform diagram showing a write operation of the DRAM cell when a first gate and a second gate are formed out of the same material;
Fig. 7B is a waveform diagram showing a write operation of the DRAM cell when the first gate and the second gate are formed out of materials with different work functions;
Fig. 7C is a diagram showing an example of the circuit configuration of a word line driver and a row decoder to generate waveforms of the write operation in Fig. 7B;
Fig. 7D is a diagram showing a modified example of the word line driver shown in Fig. 7C;
Fig. 7E is a diagram showing an example of a layout when the row decoder and the word line driver shown in Fig. 7C or Fig. 7D are disposed in relation to a memory cell array (disposed on one side);
Fig. 7F is a diagram showing an example of the layout when the row decoder and the word line driver shown in Fig. 7C or Fig. 7D are disposed in relation to a memory cell array (disposed on either side);
Fig. 7G is a diagram showing an example of the circuit configuration of a word line driver and a row decoder to generate waveforms of the write operation in Fig. 7A;
Fig. 7H is a diagram showing a modified example of the word line driver shown in Fig. 7G;
Fig. 7I is a diagram showing an example of a layout when the row decoder and the word line driver shown in Fig. 7G or Fig. 7H are disposed in relation to the memory cell array (when the row decoder and the word line driver on the right and the left side are disposed alternately for pairs of the first word line and the second word line);
Fig. 7J is a diagram showing an example of the layout when the row decoder and the word line driver shown in Fig. 7G or Fig. 7H are disposed in relation to the memory cell array (when the row decoder and the word line driver for the first word lines are disposed on one side and the row decoder and the word line driver for the second word lines are disposed on the other side);
Fig. 7K is a diagram showing an example of the circuit configuration of the row decoder and the word line driver for the first word lines when the layout shown in Fig. 7 J is adopted;
Fig. 7L is a diagram showing an example of the circuit configuration of the row decoder and the word line driver for the second word lines when the layout shown in Fig. 7 J is adopted;
Fig. 7M is a diagram showing an modified example of the word line driver shown in Fig. 7K;
Fig. 7N is a diagram showing an example of a layout of a memory chip in which a memory cell array composed of memory cells in the respective embodiments and its row decoders and word line drivers are disposed;
Fig. 8 is a diagram showing the sectional structure of a DRAM cell according to a second embodiment of the present invention;
Fig. 9 is a diagram showing the sectional structure of a DRAM cell according to a third embodiment of the present invention;
Fig. 10A is a diagram showing the layout of a DRAM cell array according to a fourth embodiment;
Fig. 10B is a sectional view taken along the line A-A' in Fig. 10A;
Fig. 10C is a sectional view taken along the line B-B' in Fig. 10A;
Fig. 11 is a diagram showing the sectional structure of a DRAM cell according to a fifth embodiment;
Fig. 12 is a diagram showing a mark forming step in a process of manufacturing the memory cell according to the first embodiment shown in Fig. 3;
Fig. 13 is a diagram showing the mark forming step in the manufacturing process;
Fig. 14 is a diagram showing a gate (G2) forming step in the manufacturing process;
Fig. 15 is a diagram showing a substrate sticking step in the manufacturing process;
Fig. 16 is a diagram showing a substrate polishing step in the manufacturing process;
Fig. 17 is a diagram showing a gate (G1) forming step in the manufacturing process;
Fig. 18 is a diagram showing a bit line forming step in the manufacturing process;
Fig. 19 is a diagram showing a mark forming step in a process of manufacturing the memory cell according to the second embodiment shown in Fig. 8;
Fig. 20 is a diagram showing the mark forming step in the manufacturing process;
Fig. 21 is a diagram showing a gate (G1) forming step in the manufacturing process;
Fig. 22 is a diagram showing a substrate sticking step in the manufacturing process;
Fig. 23 is a diagram showing a substrate polishing step in the manufacturing process;
Fig. 24 is a diagram showing an insulating film forming step in the manufacturing process;
Fig. 25 is a diagram showing a gate (G2) forming step in the manufacturing process;

ess (a sectional view taken along the line B-B' in Fig. 45A);
Fig. 49A is a diagram showing a gate (G1) forming step in the manufacturing process (a sectional view taken along the line A-A' in Fig. 45A);
Fig. 49B is a diagram showing the gate (G1) forming step in the manufacturing process (a sectional view taken along the line B-B' in Fig. 45A);
Fig. 50A is a diagram showing a planarizing step in the manufacturing process (a sectional view taken along the line A-A' in Fig. 45A);
Fig. 50B is a diagram showing the planarizing step in the manufacturing process (a sectional view taken along the line B-B' in Fig. 45A);
Fig. 51A is a diagram showing a gate (G2)-formed region boring step in the manufacturing process (a sectional view taken along the line A-A' in Fig. 45A);
Fig. 51B is a diagram showing the gate (G2)-formed region boring step in the manufacturing process (a sectional view taken along the line B-B' in Fig. 45A);
Fig. 52A is a diagram showing a gate electrode material depositing step in the manufacturing process (a sectional view taken along the line A-A' in Fig. 45A);
Fig. 52B is a diagram showing the gate electrode material depositing step in the manufacturing process (a sectional view taken along the line B-B' in Fig. 45A);
Fig. 53A is a diagram showing a gate (G2) forming step in the manufacturing process (a sectional view taken along the line A-A' in Fig. 45A);
Fig. 53B is a diagram showing the gate (G2) forming step in the manufacturing process (a sectional view taken along the line B-B' in Fig. 45A);
Fig. 54A is a diagram showing a layout of an embodiment in which shunt lines are added to the embodiment in Fig. 39A;
Fig. 54B is a sectional view taken along the line A-A' in Fig. 54A;
Fig. 54C is a sectional view taken along the line B-B' in Fig. 54A;
Fig. 55A is a sectional view taken along the line A-A' in Fig. 54A when a different structure of shunt lines is used;
Fig. 55B is a sectional view taken along the line B-B' in Fig. 54A when the different structure of shunt lines is used;
Fig. 56 is a diagram showing a memory cell structure when an n-channel type MIS transistor according to the first embodiment is modified into a p-channel type one corresponding to Fig. 3;
Fig. 57 is a diagram showing a memory cell structure when an n-channel type MIS transistor according to the second embodiment is modified into a p-channel type one corresponding to Fig. 8;
Fig. 58 is a diagram showing a memory cell structure when an n-channel type MIS transistor according to the third embodiment is modified into a p-channel type one corresponding to Fig. 9;
Fig. 59A is a diagram showing a memory cell structure when an n-channel type MIS transistor according to the fourth embodiment is modified into a p-channel type one corresponding to Fig. 10B;
Fig. 59B is a diagram showing the memory cell structure when the n-channel type MIS transistor according to the fourth embodiment is modified into the p-channel type one corresponding to Fig. 10C;
Fig. 60A is a diagram showing a memory cell structure when an n-channel type MIS transistor according to the fifth embodiment is modified into a p-channel type one corresponding to Fig. 11;
Fig. 60B is a diagram showing drive voltage waveforms when the p-type channel MIS transistor is used corresponding to Fig. 7A;
Fig. 60C is a diagram showing drive voltage waveforms when the p-type channel MIS transistor is used corresponding to Fig. 7B;
Fig. 61 is a diagram showing device parameters used for simulation of the cell in the embodiment in Fig. 3;
Fig. 62 is a diagram showing voltage waveforms of a "0" write operation and the succeeding read operation in the simulation;
Fig. 63 is a diagram showing voltage waveforms of a "1" write operation and the succeeding read operation in the simulation;
Fig. 64 is a diagram showing a drain current - gate voltage characteristic of the cell at the time of "0" and "1" data write operations in the simulation;
Fig. 65 is a diagram showing voltage waveforms of a "0" write operation and the succeeding read operation in simulation in which an auxiliary gate is set at a fixed potential;
Fig. 66 is a diagram showing voltage waveforms of a "1" write operation and the succeeding read operation in the simulation;
Fig. 67 is a diagram showing a drain current - gate voltage characteristic of the cell at the time of "0" and "1" data write operations in the simulation;
Fig. 68A is a plan view of a cell array according to a sixth embodiment;
Fig. 68B is a sectional view taken along the line I-I' in Fig. 68A;
Fig. 68C is a sectional view taken along the line II-II" in Fig. 68A;
Fig. 69 is a sectional view showing a step of forming a gate electrode material film on a first silicon substrate in a manufacturing process in the embodiment;
Fig. 70 is a sectional view showing a step of implanting hydrogen ions into a second silicon substrate in the manufacturing process;
Fig. 71 is a sectional view showing a substrate sticking step in the manufacturing process;
Fig. 72 is a sectional view showing a step of adjusting the thickness of the stuck substrate in the man-

a capacitor, non-destructive read-out is possible.

[0025] In the aforementioned basic DRAM cell structure, to what extent the difference in threshold voltage between data "0" and "1" can increase is an important point. As is obvious from the aforementioned operational principle, the write characteristic and hold characteristic of data are determined by controlling the body potential by capacitive coupling from the gate 13. However, since the threshold voltage is about the square root of the body potential, it is not easy to realize a great difference in threshold voltage between the data "0" and "1". Besides, in the aforementioned write operation, the memory cell MC during the "0" write operation performs triode operation, and hence the gate 13 and the channel body do not perform capacitive coupling when the channel is formed, whereby the body potential can not be increased.

[0026] Accordingly, in the undermentioned embodiments, as against the aforementioned basic structure of the memory cell, an auxiliary gate (a second gate) to control the body potential by capacitive coupling to the body of the MIS transistor is provided in addition to a main gate (a first gate) which is used for the formation of the channel. By driving the second gate in synchronization with the first gate, more certain data write operation is realized, and the data "0" and "1" with a great difference in threshold voltage can be stored.

[0027] Concrete embodiments will be explained below.

[First embodiment]

[0028] Fig. 3 shows the structure of a memory cell MC according to a first embodiment corresponding to the basic structure in Fig. 1. A point different from Fig. 1 is that a second gate (G2) 20 to control the body potential is provided in addition to a first gate (G1) 13 which is a front gate used for the control of the channel of the transistor. In this embodiment, the second gate 20 is buried in the oxide film 11 under the silicon layer 12 as an opposite back gate to perform capacitive coupling to a bottom face of the silicon layer 12 with a gate insulating film 19 therebetween.

[0029] Fig. 4 shows an equivalent circuit of a memory cell array in which a plurality of such memory cells MC are arranged in a matrix form. The first gates (G1) 13 of a plurality of memory cells MC arranged in one direction are connected to first word lines WL1, and the second gates (G2) 20 are connected to the second word lines WL2. Bit lines BL to which the drains of the memory cells MC are connected are disposed in a direction intersecting these word lines WL1 and WL2. The sources 15 of all the memory cells MC are connected to a fixed potential line (a ground potential line VSS).

[0030] Fig. 5 shows the layout of the memory cell array, and Fig. 6A and Fig. 6B respectively show sections taken along the line A-A' and the line B-B' in Fig. 5. The p-type silicon layer 12 is pattern-formed in a lattice form by burying a silicon oxide film 21 therein. Namely, two transistor regions sharing the drain region 14 are arranged, being device-isolated in the direction of the word lines WL 1 and WL2 by the silicon oxide film 21. Alternatively, instead of burying the silicon oxide film 21, device isolation in a crosswise direction may be performed by etching the silicon layer 12. The first gates 13 and the second gates 20 are formed continuously in one direction to constitute the word lines WL1 and WL2. The sources 15 are continuously formed in the direction of the word lines WL1 and WL2 to constitute the fixed potential line (common source line). The transistors are covered with an interlayer dielectric film 17, and bit lines (BL) 18 are formed thereon. The bit lines 18 are disposed to come in contact with the drains 14 each shared by two transistors and intersect the word lines WL 1 and WL2.

[0031] Thereby, the silicon layers 12, each being a channel body of each transistor, are isolated from each other at their bottom faces and side faces in the channel width direction by the oxide film, and isolated from each other in the channel length direction by pn junction to be maintained in a floating state.

[0032] In this memory cell array structure, if the word lines WL and the bit lines BL are formed with a pitch of a minimum feature size F, a unit cell area is $2\,F \times 2\,F = 4\,F^2$ as shown by a broken line in Fig. 5.

[0033] As described above, the memory cell array capable of dynamic storage is structured with one MIS transistor as a 1 bit memory cell MC.

[0034] Fig. 7A and Fig. 7B show voltage waveforms of the word lines WL1 and WL2 and the bit line BL at the time of a data write operation. The first word line WL1 and the second word line WL2 which form a pair are driven synchronously. Fig. 7A shows that when the same material is used for the first gate 13 and the second gate 20, the accumulation of majority carriers on the second gate 20 side of the channel body becomes possible by controlling the second gate 20 at a potential lower than the first gate 13. Meanwhile, Fig. 7B shows that when electrode materials with different work functions are used for the first gate 13 and the second gate 20, the accumulation of majority carriers on the second gate 20 side of the channel body becomes possible by applying the same potential to both of them.

[0035] In the case of Fig. 7A, at the time of a "1" data write operation, a positive potential VWL1H higher than a reference potential VSS is applied to the selected first word line WL1, and a potential VWL2H (a negative potential lower than the reference potential VSS in the illustrated example) lower than the potential VWL1H is applied to the simultaneously selected second word line WL2, and a positive potential VBLH higher than the reference potential VSS is applied to the selected bit line BL. Thereby, in the selected memory cell MC, impact ionization due to a pentode operation occurs, whereby holes are accumulated in the channel body.

[0036] In a data hold operation, a negative potential

which is a potential higher than a positive potential VCC and supplies it to the word lines WL1 and WL2.

[0049] More specifically, a row address signal RADD and a word line enabling signal WLEN are inputted to the NAND circuit C10. All the high-level row address signals RADD and high-level word line enabling signals WLEN are inputted to the word line driver WDDV1 corresponding to the selected word lines WL1 and WL2. Accordingly, an output from the NAND circuit C10 of the word line driver WDDV1 corresponding to the selected word lines WL1 and WL2 is at a low level, that is, the reference potential VSS. The output from the NAND circuit C10 is inputted to the inverter circuit C11.

[0050] This inverter circuit C11 inverts the inputted signal and outputs it. Accordingly, in the selected word line driver WDDV1, an output from the inverter circuit C11 is at a high level, that is, the positive potential VCC. The output from the inverter circuit C11 is inputted to the level shift circuit C12 and the level shift circuit C13. The output from the NAND circuit C10 is also inputted to the level shift circuit C12 and the level shift circuit C13.

[0051] Outputs from the level shift circuit C12 and the level shift circuit C13 are inputted to the output buffer circuit C14. By the level shift circuit C12 and the output buffer circuit C14, the output of VCC being ahigh-level output potential of the inverter circuit C11 is changed to VWLH which is a positive potential higher than VCC and supplied to the word lines WL1 and WL2. Moreover, by the level shift circuit C13 and the output buffer circuit C14, the output of VSS being a low-level output potential of the inverter circuit C11 is changed to VWLL which is a potential lower than VSS and supplied to the word lines WL1 and WL2.

[0052] In this embodiment, the level shift circuit C12 is composed of p-type MOS transistors PM10 and PM11 and n-type MOS transistors NM10 and NM11. Source terminals of the p-type MOS transistors PM10 and PM11 are respectively connected to supply lines of the potential VWLH, and drain terminals thereof are respectively connected to drain terminals of the n-type MOS transistors NM10 and NM11. A gate terminal of the p-type MOS transistor PM10 is connected to a node between the p-type MOS transistor PM11 and the n-type MOS transistor NM11, and a gate terminal of the p-type MOS transistor PM11 is connected to a node between the p-type MOS transistor PM10 and the n-type MOS transistor NM10.

[0053] The output from the inverter circuit C11 is inputted to a gate terminal of the n-type MOS transistor NM10, and the output from the NAND circuit C10 is inputted to a gate terminal of the n-type MOS transistor NM11. Source terminals of these n-type MOS transistors NM10 and NM11 are respectively connected to supply lines of the potential VSS.

[0054] Meanwhile, the level shift circuit C13 is composed of a p-type MOS transistors PM12 and PM13 and n-type MOS transistors NM12 and NM13. Source terminals of the p-type MOS transistors PM12 and PM 13 are respectively connected to supply lines of the potential VCC, and drain terminals thereof are respectively connected to drain terminals of the n-type MOS transistors NM12° and NM13. The output from the inverter circuit C11 is inputted to a gate terminal of the p-type MOS transistor PM12, and the output from the NAND circuit C10 is inputted to a gate terminal of the p-type MOS transistor PM13.

[0055] Agate terminal of then-type MOS transistor NM12 is connected to a node between the p-type MOS transistor PM13 and the n-type MOS transistor NM13, anda gate terminal of then-type MOS transistor NM13 is connected to a node between the p-type MOS transistor PM12 and the n-type MOS transistor NM 12. Source terminals of these n-type MOS transistors NM12 and NM13 are respectively connected to supply lines of the potential VWLL.

[0056] The output buffer circuit C14 is configured by connecting p-type MOS transistors PM14 and PM15 and n-type MOS transistors NM14 and NM15 in series.

[0057] A source terminal of the p-type MOS transistor PM14 is connected to a supply line of the potential VWLH, and a gate terminal thereof is connected to the gate terminal of the p-type MOS transistor PM11 in the pressure increase circuit C12. A drain terminal of the p-type MOS transistor PM14 is connected to a source terminal of the p-type MOS transistor PM15. The potential VSS is inputted to a gate terminal of this p-type MOS transistor PM15. Hence, the p-type MOS transistor PM 15 is a normally-on MOS transistor. A drain terminal of the p-type MOS transistor PM15 is connected to a drain terminal of the n-type MOS transistor NM14. A voltage to drive the word lines WL1 and WL2 is outputted from a node between these p-type MOS transistor PM15 and n-type MOS transistor NM14.

[0058] The potential VCC is supplied to a gate terminal of the n-type MOS transistor NM14. Hence, the n-type MOS transistor NM14 is a normally-on MOS transistor. A source terminal of the n-type MOS transistor NM14 is connected to a drain terminal of the n-type MOS transistor NM15. A gate terminal of this n-type MOS transistor NM15 is connected to the gate terminal of the n-type MOS transistor NM13 in the level shift circuit C13. A source terminal of the n-type MOS transistor NM15 is connected to a supply line of the potential VWLL.

[0059] Using the row decoder RDEC and the word line driver WDDV1 structured as above, the potentials VWLH and VWLL shown in Fig. 7B are generated and supplied to the word lines WL1 and WL2. Incidentally, in Fig. 7C, back gate connection is performed in each MOS transistor, but this is not always necessary.

[0060] The output buffer circuit C14 of this word line driver WDDV1 includes the normally-on MOS transistors PM15 and NM 14 in order that a differential voltage between the potential VWLH and the potential VWLL is not directly applied to the MOS transistors PM14 and NM15. Namely, by the normally-on MOS transistors PM15 and NM14, the differential voltage is reduced by

and WL2 at odd number positions are decoded and driven by the row decoder RDEC and the word line driver WDDV2 on the left side of the memory cell array MCA and the word lines WL1 and WL2 at even number positions are decoded and driven by the row decoder RDEC and the word line driver WDDV2 on the right side of the memory cell array MCA.

[0074] Moreover, as shown in Fig. 7J, for example, it is suitable to dispose a word line driver WDDV3 for the first word lines WL1 on the left side of the memory cell array MCA and dispose a word line driver WDDV4 for the second word lines WL2 on the right side of the memory cell array MCA. This disposition can facilitate power supply wiring. Namely, it is suitable to situate potential supply lines of the potential VWL1H and the potential VWL1L only on the left side of the memory cell array MCA where the word line driver WDDV3 for the first word lines WL1 is provided and situate potential supply lines of the potential VWL2H and the potential VWL2L only on the right side of the memory cell array MCA where theword line driver WDDV4 for the second word lines WL2 is provided.

[0075] In this layout, however, individual row decoders RDEC are needed for both the word line driver WDDV3 and the word line driver WDDV4. An example of such a word line driver WDDV3 is shown in Fig. 7K, and an example of such a word line driver WDDV4 is shown in Fig. 7L.

[0076] As shown in Fig. 7K, the word line driver WDDV3 for the first word lines WL1 comprises the level shift circuit C22 connected to the row decoder RDEC via the inverter circuit C11, the level shift circuit C23 directly connected to the row decoder RDEC, and the output buffer circuit C24. Their configurations are the same as those in the aforementioned word line driver WDDV2 in Fig. 7G.

[0077] Meanwhile, as shown in Fig. 7L, the word line driver WDDV4 for the second word lines WL1 comprises the row decoder RDEC, the inverter circuit C11, the level shift circuit C25, and the output buffer circuit C26. The configurations of the level shift circuit C25 and the output buffer circuit C26 are the same as those in the aforementioned word line driver WDDV2 in Fig. 7G. However, since the word line driver WDDV4 is disposed on the right side of the memory cell array MCA, the row decoder RDEC can not be shared with the word line driver WDDV3, and hence the row decoder RDEC and the inverter circuit C11 are additionally provided for the word line driver WDDV4.

[0078] The row address signals RADD and WLEN are inputted synchronously to the row decoder RDEC of the word line driver WDDV3 and the row decoder RDEC of WDD4, and as a result word line driving potentials synchronized at different voltage amplitudes are outputted.

[0079] Incidentally, in Fig. 7K and Fig. 7L, back gate connection is performed in each MOS transistor, but this is not always necessary. Moreover, in the word line driver WDDV3 shown in Fig. 7K, the p-type MOS transistor PM25 and the n-type MOS transistor NM24 can be omitted as shown in Fig. 7M.

[0080] Fig. 7N is a diagram showing an example of the entire layout of a memory chip MCP having the aforementioned memory cell array MCA, row decoder RDEC, and word line driver WDDV. As shown in Fig. 7N, VSS being a supply voltage on the low voltage side and VCC being a supply voltage on the high voltage side are inputted. These potentials VSS and VCC are supplied to a circuit BST composed of a group of voltage increase circuits and their drivers, and various voltages necessary for this memory chip MCP are generated. An example in which four kinds of potentials VWLH, VWLL, VBLH, and VBLL corresponding to voltage waveforms in Fig. 7B are generated is shown here. When the memory cell array MCA using voltage waveforms in Fig. 7A is used, six kinds of potentials VWL1H, VWL1L, VWL2H, VWL2L, VBLH, and VBLL are generated. The various potentials generated by this circuit BST are supplied to necessary circuits via potential supply lines. Especially, the four kinds of potentials shown in this diagram are supplied to the row decoder RDEC and the word line driver WDDV as described above.

[0081] Moreover, an address to specify a memory cell which performs a data write operation and a data read operation for the memory chip MCP is inputted to the memory chip MCP. This address is inputted to an address receiver ADRV and separated into a row address signal and a column address signal. The row address signal is supplied to the row address decoder RDEC and the column address signal is supplied to a column address decoder CDEC.

[0082] Data is inputted/outputted from a data I/O terminal. More specifically, data to be written in the memory cell array MCA is inputted from the data I/O terminal and inputted to an input receiver INRV. Then, the data is supplied to a column select gate CSG via a data driver DTDV, and the data is written in the memory cell array MCA.

[0083] Meanwhile, a signal read from the memory cell array MCA is outputted from the column select gate CSG to a sense amplifier SA, and data is detected by the sense amplifier SA. The detected data is outputted from the data I/O terminal via an output driver OTDV.

[0084] This memory chip MCP includes a control signal receiver CSRV to which various kinds of control signals are inputted. Based on the control signals inputted from the outside of the memory chip MCP, the control signal receiver CSRV generates various control signals needed within the memory chip MCP and outputs them.

[0085] Incidentally, although the layout in which the row decoder RDEC and the word line driver WDDV are provided on either side of the memory cell array MCA is illustrated in the memory chip MCP in Fig. 7N, the row decoder RDEC and the word line driver WDDV are sometimes provided only one side of the memory cell array MCA as described above.

[0086] It should be noted that the hitherto explained configurations of the word line drivers WDDV1, WDDV2,

[0101] Next, manufacturing processes corresponding to the aforementioned respective embodiments will be explained.

[Manufacturing process corresponding to First embodiment]

[0102] Fig. 12 to Fig. 18 show the process of manufacturing a DRAM cell corresponding to the first embodiment shown in Fig. 3. In this embodiment, two silicon substrates are used in order that two gates 13 and 20 are disposed above and below the silicon layer. As shown in Fig. 12, in a first silicon substrate 101, trenches 102 are worked each as an alignment mark at the outside of a cell array region. As shown in Fig. 13, an oxide film 103 is buried in each of the trenches 102. The depth of the trench 102 is more than the thickness of an SOI layer which is adjusted by shaving the silicon substrate 101 later. More specifically, as will be described later, since the silicon substrate 101 becomes the silicon layer 12 in Fig. 3, the trenches 102 are formed more deeper than the thickness of the silicon layer 12.

[0103] Thereafter, as shown in Fig. 14, the second gates 20 (G2) are pattern-formed on the silicon substrate 101 with the gate insulating film 19 therebetween so as to continue as the word line WL2. A face on which the second gates 20 is formed is covered with an insulating film such as a silicon oxide film 106 and then planarized. CMP (Chemical Mechanical Polishing) is used for planarization. Then, as shown in Fig. 15, a second silicon substrate 201 is stuck on the planarized face of the silicon oxide film 106.

[0104] Thereafter, as shown in Fig. 16, the first silicon substrate 101 is polished until an intended thickness of the SOI layer is obtained. The silicon substrate 101 thus polished becomes the silicon layer 12 in Fig. 3. On this occasion, the previously buried silicon oxide film 103 protrudes, so that it can be used as a mark for alignment with the already formed second gates 20 in the next step of forming the first gates 13.

[0105] Namely, as shown in Fig. 17, a device isolation oxide film 115 to perform device isolation in the crosswise direction is buried in the silicon substrate 101 by an STI method, and thereafter the first gates (G1) 13 are pattern-formed to continue as the word line WL1 with the gate insulating film 16 therebetween. The device isolation insulating film 115 is shown only in the bit line direction in this diagram, but the device isolation insulating films 115 are formed at predetermined intervals also in the word line direction so that the silicon layer 12 isolated from others is formed in each memory cell MC region. Further, ion implantation is performed to form the drain region 14 and the source region 15. Then, as shown in Fig. 18, the interlayer dielectric film 17 is formed, and the bit lines 18 are formed thereon.

[Manufacturing process corresponding to Second embodiment]

[0106] Fig. 19 to Fig. 26 show the process of manufacturing a DRAM cell corresponding to the second embodiment shown in Fig. 8. Also in this embodiment, two silicon substrates are used in order that two gates 13 and 20 are disposed above and below the silicon layer. As shown in Fig. 19, in the first silicon substrate 101, the trenches 102 are worked each as an alignment mark at the outside of a cell array region. As shown in Fig. 20, the oxide film 103 is buried in each of the trenches 102. The depth of the trench 102 is more than the thickness of an SOI layer which is adjusted by shaving the silicon substrate 101 later. More specifically, as will be described later, since the silicon substrate 101 becomes the silicon layer 12 in Fig. 8, the trenches 102 are formed more deeper than the thickness of the silicon layer 12.

[0107] Thereafter, as shown in Fig. 21, the first gates 13 (G1) are pattern-formed on the silicon substrate 101 with the gate insulating film 16 therebetween so as to continue as the word line WL1. A face on which the first gates 13 are formed is covered with the insulating film such as the silicon oxide film 106 and then planarized. CMP (Chemical Mechanical Polishing) is used for planarization. Then, as shown in Fig. 22, the second silicon substrate 201 is stuck on the planarized face of the silicon oxide film 106.

[0108] Thereafter, as shown in Fig. 23, the first silicon substrate 101 is polished until an intended thickness of the SOI layer is obtained. The silicon substrate 101 thus polished becomes the silicon layer 12 in Fig. 8. On this occasion, the previously buried silicon oxide film 103 protrudes, so that it can be used as a mark for alignment with the already formed first gates 13 in the next step of forming the second gates 20.

[0109] As shown in Fig. 24, after the device isolation oxide film 115 is buried in the silicon substrate 101 the thickness of which is adjusted, a silicon oxide film 203 is deposited therein, and an opening 204 is made at a position corresponding to the channel body of the transistor. The device isolation insulating film 115 is shown only in the bit line direction in this diagram, but the device isolation insulating films 115 are formed at predetermined intervals also in the word line direction so that the silicon layer 12 isolated from others is formed in each memory cell MC region. Then, as shown in Fig. 25, the relay electrode 25 connected to the channel body via the opening is formed, and the second gate 20 (G2) is formed thereon with the capacitor insulating film 26 therebetween. The relay electrode 25 and the second gate 20 can be patterned integrally as the word line WL2 after being formed continuously with the capacitor insulating film 26 therebetween. With the second gate 20 as a mask, ions are implanted in the silicon layer 12 from above the silicon oxide film 203 to form the drain region 14 and the source region 15. Thereafter, as shown in Fig. 26, the interlayer dielectric film 17 is formed, and

connect the drains 18.

[Cell array and manufacturing process corresponding to Fifth embodiment]

[0121] Fig. 39A shows the layout of a concrete cell array with the DRAM cells shown in Fig. 11, Fig. 39B shows its section taken along the line A-A', and Fig. 39C shows its section taken along the line B-B'. The first gate 13 and the second gate 20 are respectively formed using the same material on both sides of the pillar silicon portion 30. These gates 13 and 20 are patterned continuously in one direction to constitute the first word lines WL1 and the second word lines WL2.

[0122] Fig. 40A, Fig. 40B to Fig. 44A, and Fig. 44B are diagrams explaining a manufacturing process by the use of sections corresponding to Fig. 39B and Fig. 39C. As shown in Fig. 40A and Fig. 40B, an n-type layer which becomes the source region 15 is previously formed on the silicon substrate 10. A p-type silicon layer 400 is epitaxially grown on this n-type layer. A mask of a silicon nitride film 401 is pattern-formed on such an epitaxial substrate, stripe-shaped trenches continuing in the bit line direction are worked by etching the silicon layer 400, and a device isolation oxide film 402 is buried in each of the trenches.

[0123] Further, in another example, the epitaxial growth method is not used, but the n-type layer which becomes the source region 15 may be formed by implanting ions in a normal p-type silicon substrate.

[0124] As shown in Fig. 41A and Fig. 41B, the silicon nitride film 401 is changed into a pattern in which it is separated also in the bit line direction. With this silicon nitride film 401 as a mask, the silicon layer 400 in a stripe form is etched again. Thus, the silicon layer 400 is separated both in the bit line direction and the word line direction, and the pillar silicon portions 30 separated from each other are obtained in respective memory cell MC regions.

[0125] Subsequently, after portions of the device isolation oxide film 402 corresponding to regions where the word lines are buried are selectively etched, the silicon nitride film 401 is removed, and as shown in Fig. 42A and Fig. 42B, a gate insulating film 403 (corresponding to the gate insulating films 16 and 19 in Fig. 11) is formed around the pillar silicon portions 30, and a polycrystalline silicon film 404 is deposited.

[0126] Then, as shown in Fig. 43A and Fig. 43B, the polycrystalline silicon film 404 is etched by RIE to form the first gates 13 and the second gates 2 continuing as the word lines WL1 and WL2. Namely, the gates 13 and 20 are formed by etching the polycrystalline silicon film 404 by sidewall leaving technology.

[0127] Thereafter, as shown in Fig. 44A and Fig. 44B, the n-type drain region 14 is formed on the top of the pillar silicon portion 30 by ion implantation. Subsequently, a silicon oxide film 405 is deposited and then planarized. Thereafter, as shown in Fig. 39B and Fig. 39C, the interlayer dielectric film 17 is deposited, and contact holes are bored therein to form the bit lines 18.

[Another cell array and its manufacturing process corresponding to Fifth embodiment]

[0128] In Fig. 39A and Fig. 39B, the same electrode material is used for the first gate 13 and the second gate 20, but Fig. 45A to Fig. 45C show a structure when different electrode materials are used for the first gate 13 and the second gate 20 in the same cell array structure, corresponding to Fig. 39A to Fig. 39C.

[0129] As in the case of Fig. 39A to Fig. 39C, the first gate (G1) 13 and the second gate (G2) are respectively formed on both sides of the pillar silicon portion 30 with the gate insulating films 16 and 19 therebetween. However, they are different in that the first gate 13 and the second gate 20 are put in the reverse disposition alternately in the memory cells MC adjoining in the direction of the bit line BL due to the use of different materials for these gates 13 and 20. Namely, the first word line WL1 and the second word line WL2 are formed in different processes and two lines each are alternately arranged between the pillar silicon portions 30.

[0130] Fig. 46A, Fig. 46B to Fig. 53A, and Fig. 53B are diagrams explaining its manufacturing process corresponding to sections in Fig. 45B and Fig. 45C. As shown in Fig. 46A and Fig. 46B, an n-type layer which becomes the source region 15 is previously formed on the entire surface of the silicon substrate 10. The p-type silicon layer 400 is epitaxially grown on this n-type layer. A mask of the silicon nitride film 401 is pattern-formed on such an epitaxial substrate, stripe-shaped trenches continuing in the bit line direction are worked by etching the silicon layer 400, and the device isolation oxide film 402 is buried in each of the trenches.

[0131] Further, in another example, the epitaxial growth method is not used, but the n-type layer which becomes the source region 15 may be formed by implanting ions in a normal p-type silicon substrate.

[0132] As shown in Fig. 47A and Fig. 47B, the silicon nitride film 401 is modified into a pattern in which it is separated also in the bit line direction. With this silicon nitride film 401 as a mask, the silicon layer 400 in a stripe form is etched again. Thus, the silicon layer 400 is separated both in the bit line direction and the word line direction and left as the pillar silicon portions 30 separated from each other in respective memory cell MC regions.

[0133] Subsequently, after portions of the device isolation oxide film 402 corresponding to regions where the word lines are buried are selectively etched, the silicon nitride film 401 is removed, and as shown in Fig. 48A and Fig. 48B, the gate insulating film 16 is formed around the pillar silicon portions 30, and the polycrystalline silicon film 404 is deposited. This polycrystalline silicon film 404 is etched by RIE to form the first gates 13 continuing as the word lines WL1 as shown in Fig. 49A and Fig. 49B. Namely, the first gates 13 are formed

hold operation (the point in time t5) is -0.6 V.

[0147] The aforementioned results reveal that the potential difference of channel body between data "0" and "1" is 1 V, and that the data read operation is possible by using threshold difference due to this substrate bias effect. Fig. 64 shows the relation between a drain current Ids and a gate voltage Vgs at the time of the "0" and "1" data read operations. The threshold of the "1" data is Vth1 = 1.6 V, and the threshold of the "0" data is Vth0 = 1.9 V, whereby a threshold difference ΔVth = 300 mV is obtained.

[0148] An important point of the aforementioned cell operations is whether the data of the selected cell can be inverted from "1" to "0" without the "1" data of the non-selected cells (which maintain the main gate at 0 V and the auxiliary gate at -1.5 V) connected to the selected bit line (VBL = -1.5 V) being destroyed at the time of the "0" write operation. The necessary condition therefor is that the channel body potential of the "1" data cell in the hold state is equal to or lower than the channel body potential of the "0" write operation data cell. In the aforementioned example, the body potential of the "1" data cell is -0.6 V in the hold state, while the body potential at the time of the "0" data write operation (a point in time t3) is -0.75 V, and hence it is reversed slightly (0.15 V), but it does not cause data destruction.

[0149] The reason why the auxiliary gate G2 is varied in synchronization with the main gate G1 with an offset of 2 V is that capacitive coupling of each gate to the channel body is made larger than that in the case of the main gate G1 only or in the case where the auxiliary gate G2 has a fixed potential, thereby improving the following characteristic of the channel body to the gate and lowering the channel bodies of non-selected "1" data cells along the selected bit line to a level at which they are not destroyed. Thereby, the hold level of the main gate G1 can be at 0 V, and the word line amplitude can be kept below 2 V.

[0150] For reference, the result of simulation of the "0" write operation and the "1" write operation when the auxiliary gate G2 is set at a fixed potential (VWL2 = -1.5 V) is shown in Fig. 65, Fig. 66, and Fig. 67 corresponding to Fig. 62, Fig. 63, and Fig. 64. The main gate G1 has an amplitude of VWL1 = -2.5 V to 2 V.

[0151] From this result, when the auxiliary gate G2 is fixed, the channel body potential of the "1" data can not be lowered to - 0.7 V unless the main gate G1 is lowered to - 2.5 V at the time of the data hold operation. Accordingly, varying the potential of the auxiliary gate in synchronization with that of the main gate is effective in reducing the voltage.

[0152] The case where both the main gate G1 and the auxiliary gate G2 are made of p^+-type polycrystalline silicon is explained above, but n^+-type polycrystalline silicon also can be used. Especially, Th use of the n^+-type polycrystalline silicon only on the main gate G1 side is desirable in further reducing the voltage. Namely, if the main gate G1 is made of the n^+-type polycrystalline silicon, the potential of the main gate G1 is shifted to the negative side by 1 V. At the time of the "0" write operation, the bit line is - 1.5 V, and hence the gate-drain maximum voltage is 2.5 V. If the bit line potential at the time of the "0" write operation can be increased to -1 V, the maximum voltage applied to the gate insulating film becomes 2.0 V, resulting in a reduction in voltage.

[Cell array and manufacturing process in Sixth embodiment]

[0153] Although the cell array with a cell area of 4 F^2 is briefly explained in the first embodiment in Fig. 3 to Fig. 6, the sixth embodiment which further embodies the first embodiment will be explained next. Fig. 68A is a layout of a cell array according to the sixth embodiment, Fig. 68B shows its sectional view taken along the line I-I', and Fig. 68C is its sectional view taken along the line II-II'.

[0154] In this embodiment, a memory cell array composed of MIS transistors each with a double gate structure is made using stuck substrates of two silicon substrates 601 and 701. The auxiliary gates (G2) 20 are formed as the word lines WL2 each continuing in one direction on a surface of a first silicon substrate 601 with an insulating film 602 of a silicon oxide film layer therebetween. However, the auxiliary gates 20 are pattern-formed after the silicon substrate 601 has been stuck in a state in which a gate electrode material film was formed over the entire surface. These auxiliary gates 20 are isolated by insulating films 803 and 804.

[0155] The second silicon substrate 701 is stuck in a state in which the gate insulating film 19 is formed on surfaces of the auxiliary gates 20. The thickness of the silicon substrate 701 is adjusted after it is stuck, and stripe-shaped device-formed regions each continuing in the bit line direction are demarcated. In each of the device-formed regions, the main gate (G1) 13 is pattern-formed as the word line WL1 continuing in parallel with the auxiliary gate 20 with the gate insulating film 16 therebetween. Although its concrete process will be explained later in detail, trenches to isolate the auxiliary gates 20 are formed after the substrate is stuck, an insulating film and a semiconductor layer are buried in each of the isolation trenches, and then the auxiliary gates 20 and the self-aligned main gates 13 are buried.

[0156] The upper face and side faces of the main gate 13 are covered with silicon nitride films 809 and 807 each being a protective film with a selective etching ratio larger than the interlayer dielectric film and the like. The drain and source diffusion regions 14 and 15 are formed in space portions between the main gates 13. The source diffusion region 15 is baked with a source line 902 which is parallel to the word lines WL1 and WL2. An interlayer dielectric film 900 such as a silicon oxide film or the like is formed on a face on which the source lines 902 are formed, and the bit lines (BL) 18 coming into contact with the drain diffusion regions 14 are

fusion regions 14 are formed at intervals in the word line direction, and the source diffusion regions 15 continue in the word line direction to become a common source line. However, it is suitable to form the aforementioned device isolation insulating film 905 also in each of the source diffusion regions 15, whereby the source diffusion regions 15 are formed at intervals in the word line direction similarly to the drain diffusion regions 14.

[0168] Subsequently, as shown in Fig. 87, an interlayer dielectric film 900a such as a silicon oxide film is deposited. As shown in Fig. 88, stripe-shaped wiring trenches 901 each continuing in the word line direction are formed at positions corresponding to the source diffusion regions 15 of the interlayer dielectric film 900a by lithography and etching. Then, the source lines 902 are buried in the respective wiring trenches 901 by deposition of a polycrystalline silicon film and etching as shown in Fig. 89. Thanks to this source lines 902, the resistance of the source diffusion regions 15 is lowered when being formed continuously, and when the source diffusion regions are formed at intervals, they are connected jointly.

[0169] Thereafter, as shown in Fig. 90, an interlayer dielectric film 900b such as an silicon oxide film is deposited. After trenches to bury the bit lines and contact holes 903 are formed by the dual damascene method as shown in Fig. 91, the bit lines 18 are buried as shown in Fig. 68B.

[0170] As described above, according to this embodiment, by the use of the bonded SOI substrate, the main gates 13 and the auxiliary gates 20 above and below the MIS transistors can be pattern-formed as the word lines WL1 and WL2 while being self-aligned. If the word lines WL1 and WL2 and the bit lines BL are formed with the width and pitch of a minimum feature size F, a cell array having a unit cell area of 4 F^2 is obtained as shown by the alternate long and short dash line in Fig. 68A. Moreover, the upper face and side faces of each of the main gates 13 are covered with the silicon nitride films 809 and 807, and hence the source lines 902 buried in the interlayer dielectric film 902a are self-aligned with the main gates 13 covered with the silicon nitride films and can be brought into contact with the source diffusion regions 15. The contact of the bit lines is also self-aligned with the main gates 13. Accordingly, the DRAM cell array with high reliability with a micro-transistor structure can be obtained.

[0171] As shown in Fig. 68B, the source line 902 is not covered with a protective film in this embodiment. The main gate 13 is covered with the silicon nitride films 809 and 807, and therefore when the bit line contact hole is formed in the interlayer dielectric film, the bit line contact hole can be self-aligned with the main gate 13 by the selective etching ratio of the interlayer dielectric film made of the silicon oxide film to the silicon nitride film. When the contact hole is made large, however, there is a possibility that a short circuit occurs between the bit line and the source line 902 by misalignment. To prevent this, it is preferable to cover the source line 902 also with a protective film such as a silicon nitride film.

[0172] Such a preferable structure is shown in Fig. 92 corresponding to Fig. 68B. The upper face and side faces of the source line 902 are covered with a silicon nitride film 905. In order to obtain this concrete structure, the following method is recommended instead of the burying method of the source lines 902 explained in Fig. 87 to Fig. 89. Specifically, in the state of Fig. 86, a laminated film of a polycrystalline silicon film and a silicon nitride film is deposited, and the source lines 902 are formed by pattern-forming the laminated film. Subsequently, a silicon nitride film is formed on each side face of the source line 902. Thus, the source line 902 covered with the silicon nitride film can be obtained.

[0173] Fig. 92 shows an example in which a bit line forming step is also different from that in the above embodiment. Specifically, the interlayer dielectric film 900 is deposited, the bit line contact holes are formed therein, and contact plugs 906 made of polycrystalline silicon or the like are buried. Thereafter the bit lines 18 are formed.

[0174] By covering the source line 902 with the silicon nitride film 905 as above, a short circuit between the bit line and the source line 902 is prevented even if the position of the bit line contact hole slightly deviates in the burying step of the contact plug 906. Accordingly, it is possible to make the bit line contact hole large and certainly bring the bit line 18 into contact with the drain diffusion region 14 at low resistance.

[Modified example of the aforementioned embodiments]

[0175] Although the DRAM cell is composed of the n-channel type MIS transistor in the embodiments heretofore, a p-channel type MIS transistor can be used instead. For example, a cell structure when the p-channel type transistor is used is shown in Fig. 56 corresponding to Fig. 3. A portion of the p-type silicon layer 12 becomes an n-type silicon layer 12a, and p-type drain diffusion region 14a and source diffusion region 15a are formed therein. similarly, p-channel DRAM cell structures corresponding to Fig. 8, Fig. 9, Fig. 10B and Fig. 10C, and Fig. 11 are shown in Fig. 57, Fig. 58, Fig. 59A and Fig. 59B, and Fig. 60A respectively.

[0176] It is recommended that the potential relation in write and read operations and the like when the p-channel type DRAM cell is used be reversed relative to the case of the n-channel type one with the fixed potential line to which the source is connected as a reference potential. An example of concrete voltage waveforms is shown in Fig. 60B and Fig. 60C corresponding to the above Fig. 7A and Fig. 7B.

[0177] Specifically, as shown in Fig. 60B, when the first word line WL1 and the second word line WL2 are formed out of the same material, at the time of a "1" data write operation, a potential VWL1L lower than a reference potential VSS is applied to the selected first word line WL1, and a potential VWL2L (a positive potential

wherein the main gate (13) is provided between the semiconductor substrate (10) and the semiconductor layer (12), and

the auxiliary gate (20) and the relay electrode (25) are provided opposite to the main gate with the semiconductor layer (12) therebetween.

6. The semiconductor memory device according to claim 4,

wherein the auxiliary gate (20) and the relay electrode (25) are provided between the semiconductor substrate (10) and the semiconductor layer (12), and

the main gate (13) is provided opposite to the auxiliary gate (20) and the relay electrode (25) with the semiconductor layer (12) therebetween.

7. The semiconductor memory device according to claim 1,

wherein the semiconductor layer (12) is formed on a semiconductor substrate (10) with an insulating film (11) therebetween,

the main gates (13) making a pair are provided to face each other on both side faces of the channel body in the semiconductor layer, and
the auxiliary gate (20) is formed on an upper face of the semiconductor layer and electrically connects the main gates (13) making the pair.

8. The semiconductor memory device according to claim 1,

wherein the semiconductor layer (12) is a pillar semiconductor portion (30) formed on a semiconductor substrate,

the drain region (14) is formed on the pillar semiconductor portion,
the source region (15) is formed under the pillar semiconductor portion, and
the main gate (13) and the auxiliary gate (20) are provided to face each other on both side faces of the pillar semiconductor portion.

9. The semiconductor memory device according to claim 8, wherein the main gate (13) and the auxiliary gate (20) are formed out of the same material.

10. The semiconductor memory device according to claim 8, wherein the main gate (13) and the auxiliary gate (20) are formed out of different materials.

11. The semiconductor memory device according to claim 8,

wherein the MIS transistors are arranged in a matrix form to constitute a memory cell array (MCA),

the main gates (13) of the MIS transistors arranged in a first direction are continuously formed to constitute first word lines,
the auxiliary gates (20) of the MIS transistors arranged in the first direction are continuously formed to constitute second word lines,
an interlayer dielectric film (409) to cover the first word lines and the second word lines is formed,
first shunt lines (500) are formed along the first direction on the interlayer dielectric film and contacts the first word lines, and
second shunt lines (500) are formed along the first direction on the interlayer dielectric film and contacts the second word lines.

12. The semiconductor memory device according to claim 11, wherein the first shunt lines (500) and the second shunt lines (500) are formed out of the same material.

13. The semiconductor memory device according to claim 11, wherein the first shunt lines (500a) and the second shunt lines (500b) are formed out of different materials.

14. The semiconductor memory device according to claim 1, wherein the main gate and the auxiliary gate are formed out of the same material and driven synchronously at different potentials.

15. The semiconductor memory device according to claim 14, comprising:

a row decoder (RDEC) which decodes an inputted row address signal and outputs a decode result signal indicating whether a row address of the row address signal coincides or not, the decode result signal having a first control potential (VSS) or a second control potential (VCC) higher than the first control potential based on its decode result;
a first output circuit (C22, C23, C24) to which the decode result signal is inputted and which outputs a third control potential (VWL1L) lower than the first control potential or a fourth control potential (VWL1H) higher than the second control potential to the main gate based on the decode result indicated by the decode result signal; and
a second output circuit (C25, C26) to which the decode result signal is inputted and which outputs a fifth control potential (VWL2H) lower than the third control potential or a sixth control potential (VWL2L) lower than the fourth control potential to the auxiliary gate based on the decode result indicated by the decode result signal.

make pairs with the first word lines,
the main gates (13) of the MIS transistors arranged in the first direction are respectively connected to one of the first word lines,
the auxiliary gates (20) of the MIS transistors arranged in the first direction are respectively connected to one of the second word lines,
the row decoders (RDEC) and the output circuits (C12, C13, C14) for the first and second word lines which make pairs at odd number positions are provided on one side of the memory cell array, and
the row decoders (RDEC) and the output circuits (C12, C13, C14) for the first and second word lines which make pairs at even number positions are provided on the other side of the memory cell array.

23. The semiconductor memory device according to claim 1,

wherein the MIS transistors are n-channel type and arranged in a matrix form, the drain regions (14) of the MIS transistors arranged in a first direction are respectively connected to one of bit lines (BL), the main gates (13) of the MIS transistors arranged in a second direction are respectively connected to one of first word lines (WL1), the auxiliary gates (20) of the MIS transistors arranged in the second direction are respectively connected to one of second word lines (WL2), and the source regions (15) of the MIS transistors are connected to a fixed potential line to thereby constitute a memory cell array,

wherein at the time of a data write operation, with the fixed potential line as a reference potential, a first control potential (VWL1H) higher than the reference potential is applied to a selected first word line, a second control potential (VWL1L) lower than the reference potential is applied to non-selected first word lines, a third control potential (VBLH) higher than the reference potential and a fourth control potential (VBLL) lower than the reference potential are applied to the bit line according to the first and second data states, a fifth control potential (VWL2H) lower than the first control potential is applied to a second word line selected simultaneously with the first word line, and a six control potential (VWL2L) lower than the second control potential is applied to non-selected second word lines.

24. The semiconductor memory device according to claim 1,

wherein the MIS transistors are p-channel type and arranged in a matrix form, the drain regions (14a) of the MIS transistors arranged in a first direction are respectively connected to one of bit lines (BL), the main gates (13) of the MIS transistors arranged in a second direction are respectively connected to one of first word lines, the auxiliary gates (20) of the MIS transistors arranged in the second direction are respectively connected to one of second word lines, and the source regions (15a) of the MIS transistors are connected to a fixed potential line to thereby constitute a memory cell array,

wherein at the time of a data write operation, with the fixed potential line as a reference potential, a first control potential (VWL1L) lower than the reference potential is applied to a selected first word line, a second control potential (VWL1H) higher than the reference potential is applied to non-selected first word lines, a third control potential (VBLL) lower than the reference potential and a fourth control potential (VBLH) higher than the reference potential are applied to the bit line according to the first and second data states, a fifth control potential (VWL2L) higher than the first control potential is applied to a second word line selected simultaneously with the first word line, and a six control potential (VWL2H) higher than the second control potential is applied to non-selected second word lines.

25. A semiconductor memory device having MIS transistors to constitute memory cells (MC), each of the MIS transistors having a first data state and a second data state, the semiconductor memory device, comprising:

a first semiconductor substrate (601);
auxiliary gates (20) of the MIS transistors formed on the first semiconductor substrate to continue in one direction while their bottom faces and side faces are covered with an insulating film (602, 803);
a second semiconductor substrate (701) provided on the auxiliary gates with a first gate insulating film (19) therebetween;
main gates (13) of the MIS transistors formed on the second semiconductor substrate with a second gate insulating film (807, 809) to continue in parallel with the auxiliary gates;
source regions (15) formed in space portions between the main gates and the auxiliary gates in the second semiconductor substrate;
drain regions (14) formed apart from the source regions in space portions between the main gates and the auxiliary gates in the second semiconductor substrate;
source lines (902) provided to be in contact with the source regions and continue in parallel with the main gates and the auxiliary gates;
an interlayer dielectric film (900) covering the source lines; and
bit lines (18) formed on the interlayer dielectric film in a direction intersecting the main gates and the auxiliary gates and being in contact with the drain regions.

ory device, comprising:

forming a gate electrode material film (603) on a first semiconductor substrate (601) with a first insulating film (602) therebetween;

bonding a second semiconductor substrate (701) on the gate electrode material film with a first gate insulating film (19) therebetween;

forming a device isolation insulating film (704) in the second semiconductor substrate to demarcate device-formed regions continuing in a first direction in a stripe form;

depositing a second insulating film (801) on the second semiconductor substrate where the device-formed regions are demarcated and pattern-forming the second insulating film as dummy gates continuing in a second direction orthogonal to the first direction;

etching the second semiconductor substrate (701), the first gate insulating film (19), and the gate electrode material film (603) sequentially with the dummy gates as a mask to form auxiliary gates (20) out of the gate electrode material film to continue in the second direction;

burying a third insulating film (804) halfway in a thickness direction of the second semiconductor substrate in a space between the dummy gates;

forming a semiconductor layer (805) on the third insulating film in the space between the dummy gates so that side faces thereof touch the second semiconductor substrate (701);

removing the dummy gates and forming a second gate insulating film (16) on a surface of the exposed second semiconductor substrate (701);

burying main gates (13) continuing in parallel with the auxiliary gates in space portions in the semiconductor layer;

ion-implanting impurities into the semiconductor layer to form source regions (15) and drain regions (14);

forming source lines (902) being in contact with the source regions (15) and continuing in the second direction; and

forming an interlayer dielectric film (900b) covering the source lines and forming bit lines (18) being in contact with the drain regions (14) and continuing in the first direction on the interlayer dielectric film.

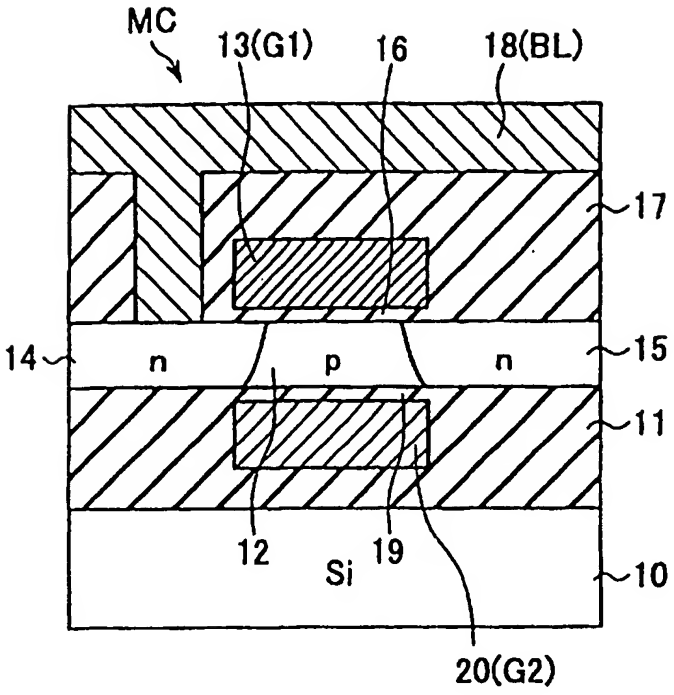
MC
13(G1)
16
18(BL)
17
14
n
p
n
15
11
12
Si
19
10
20(G2)

FIG. 3

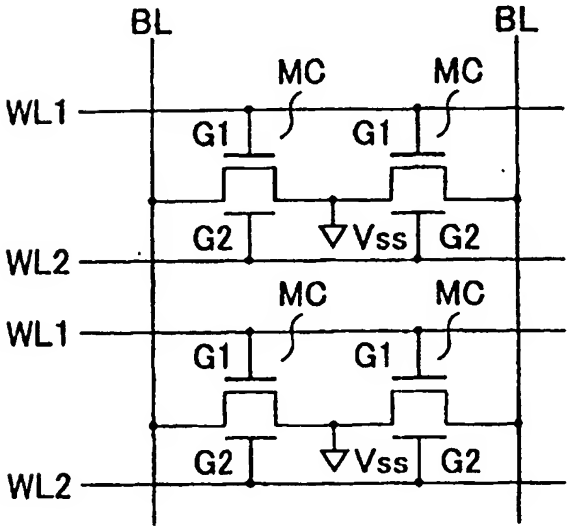
BL
BL
MC
MC
WL1
G1
G1
G2
Vss
G2
WL2
MC
MC
WL1
G1
G1
G2
Vss
G2
WL2

FIG. 4

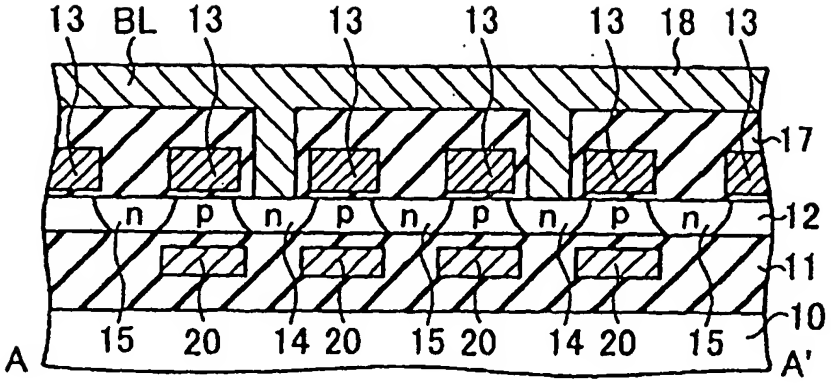
13
BL
13
13
13
13
18
13
17
n
p
n
p
n
p
n
p
n
12
11
10
15
20
14
20
15
20
14
20
15
A
A'

FIG. 6A

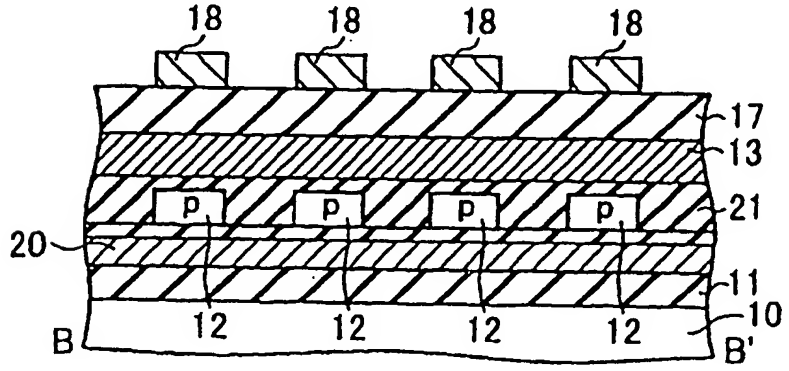
18
18
18
18
17
13
p
p
p
p
21
20
11
10
12
12
12
12
B
B'

FIG. 6B

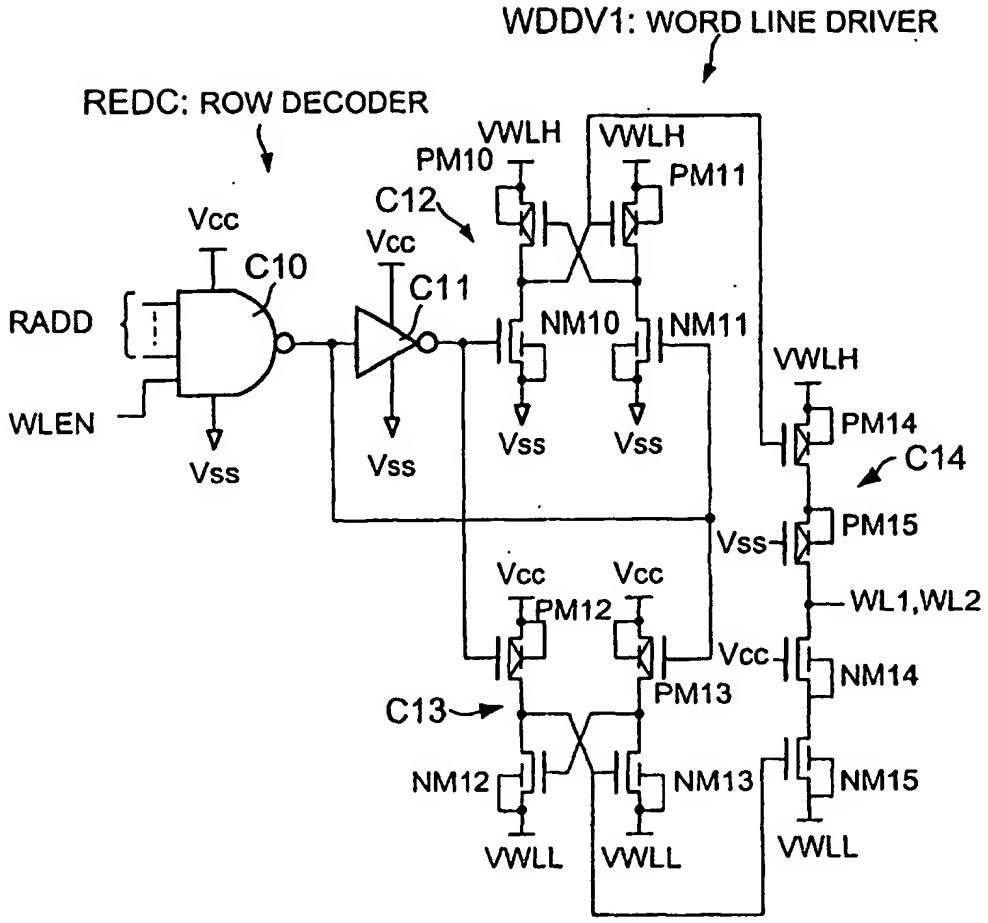
WDDV1: WORD LINE DRIVER
REDC: ROW DECODER
VWLH
VWLH
PM10
PM11
C12
Vcc
Vcc
C10
C11
RADD
NM10
NM11
VWLH
WLEN
PM14
C14
Vss
Vss
Vss
Vss
PM15
Vss
Vcc
Vcc
PM12
WL1,WL2
Vcc
NM14
PM13
C13
NM12
NM13
NM15
VWLL
VWLL
VWLL

FIG. 7C

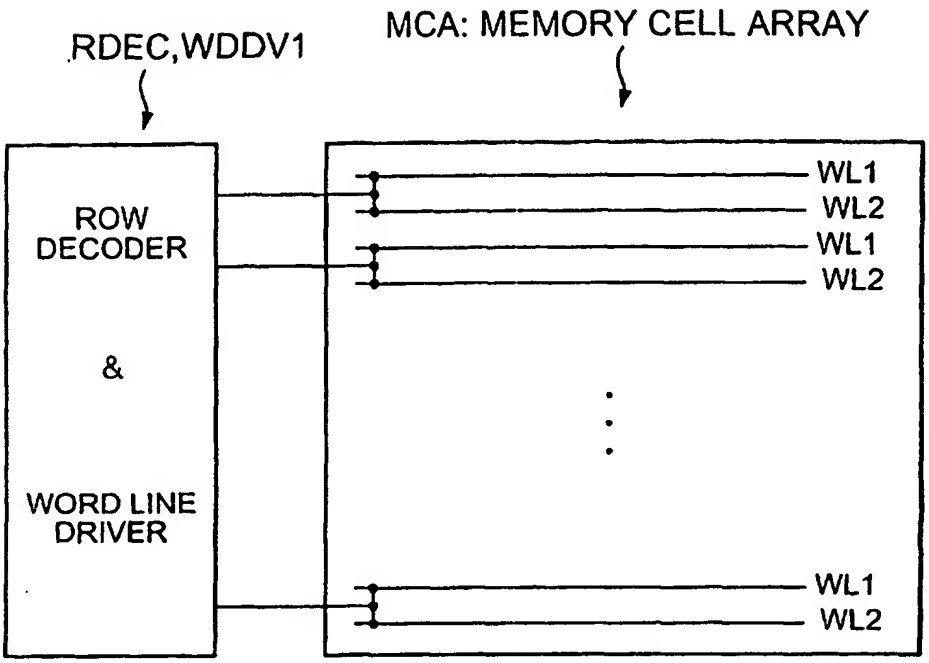
RDEC,WDDV1
MCA: MEMORY CELL ARRAY
ROW DECODER
&
WORD LINE DRIVER
WL1
WL2
WL1
WL2
WL1
WL2

FIG. 7E

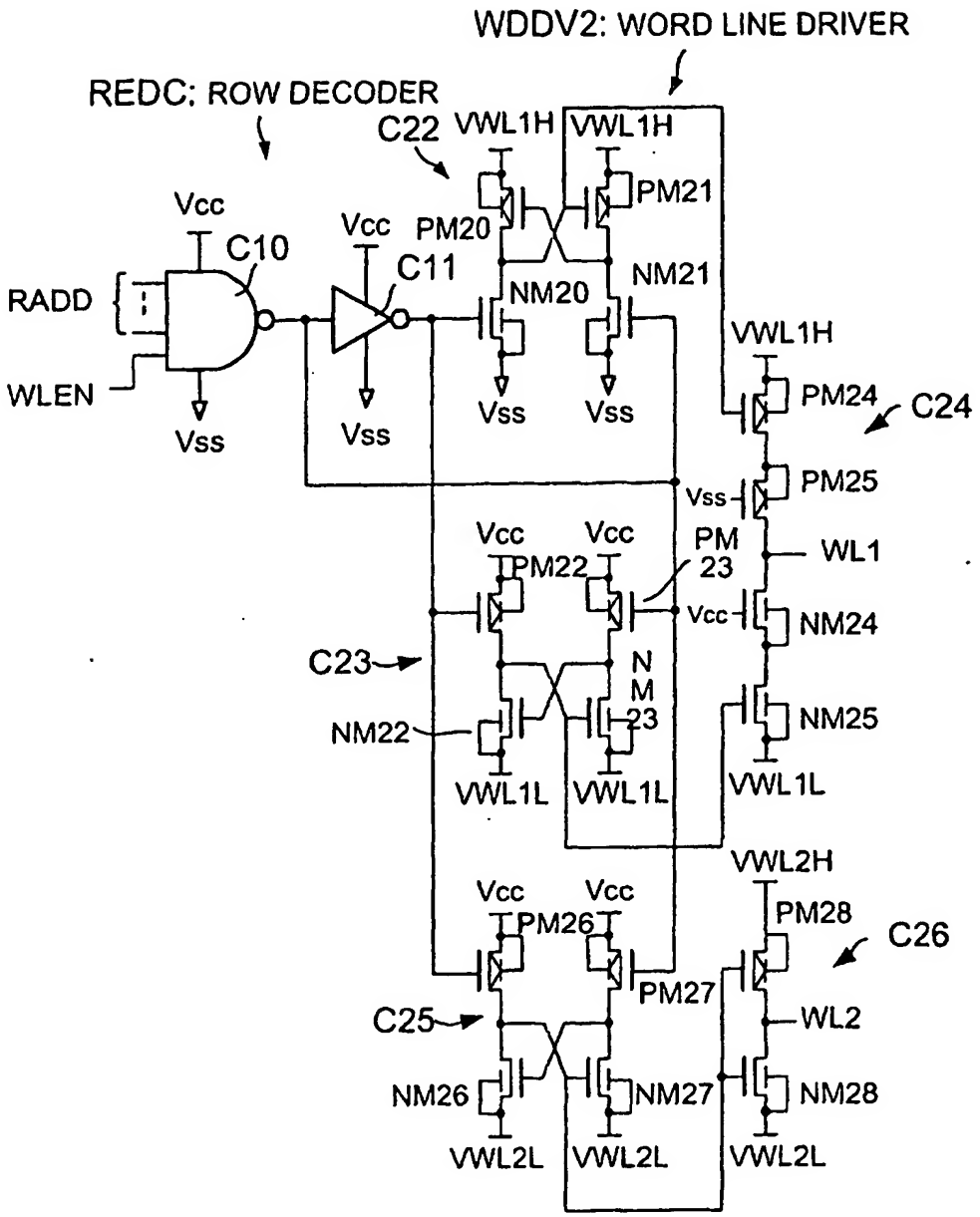
WDDV2: WORD LINE DRIVER
REDC: ROW DECODER
C22
VWL1H
VWL1H
PM21
Vcc
C10
Vcc
PM20
C11
NM21
NM20
RADD
VWL1H
WLEN
PM24
C24
Vss
Vss
Vss
Vss
PM25
Vss
Vcc
Vcc
PM
23
WL1
PM22
Vcc
NM24
C23
N
M
23
NM22
NM25
VWL1L
VWL1L
VWL1L
VWL2H
Vcc
Vcc
PM28
C26
PM26
PM27
C25
WL2
NM26
NM27
NM28
VWL2L
VWL2L
VWL2L

FIG. 7G

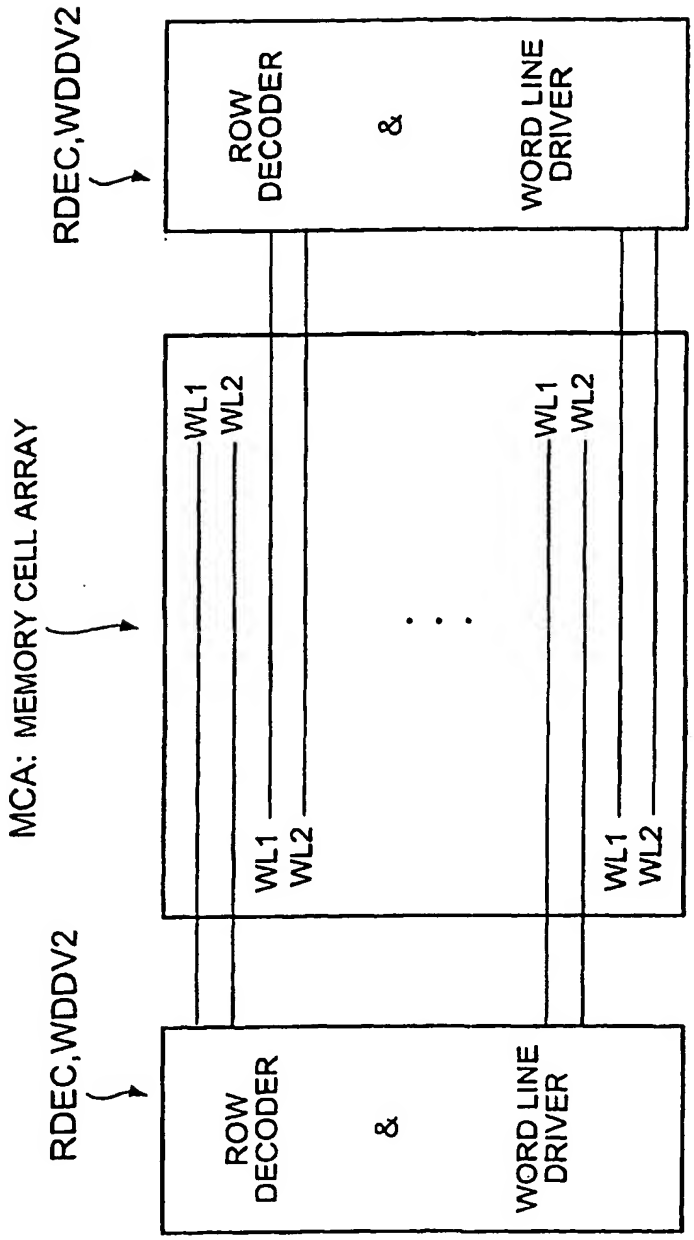
RDEC,WDDV2
ROW DECODER
&
WORD LINE DRIVER
MCA: MEMORY CELL ARRAY
WL1
WL2
WL1
WL2
WL1
WL2
WL1
WL2
RDEC,WDDV2
ROW DECODER
&
WORD LINE DRIVER

FIG. 7I

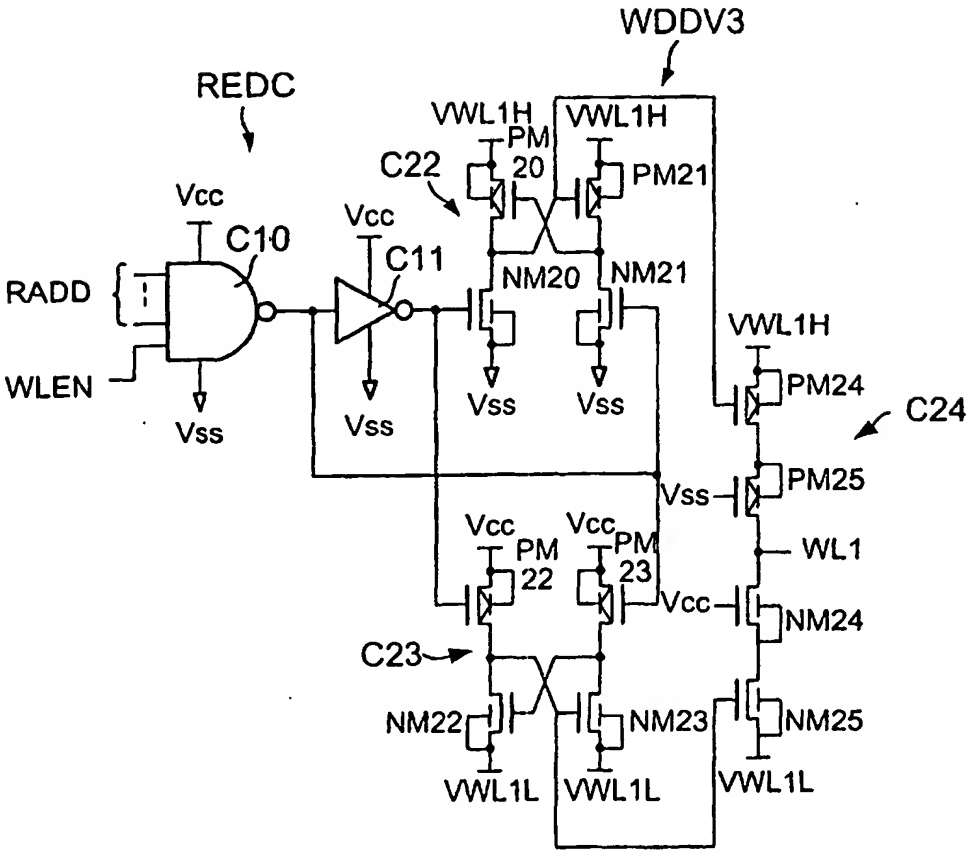
WDDV3
REDC
VWL1H
VWL1H
PM
20
PM21
C22
Vcc
Vcc
C10
C11
RADD
NM20
NM21
WLEN
VWL1H
PM24
C24
Vss
Vss
Vss
Vss
PM25
Vss
Vcc
Vcc
PM
PM
WL1
22
23
Vcc
NM24
C23
NM22
NM23
NM25
VWL1L
VWL1L
VWL1L

FIG. 7K

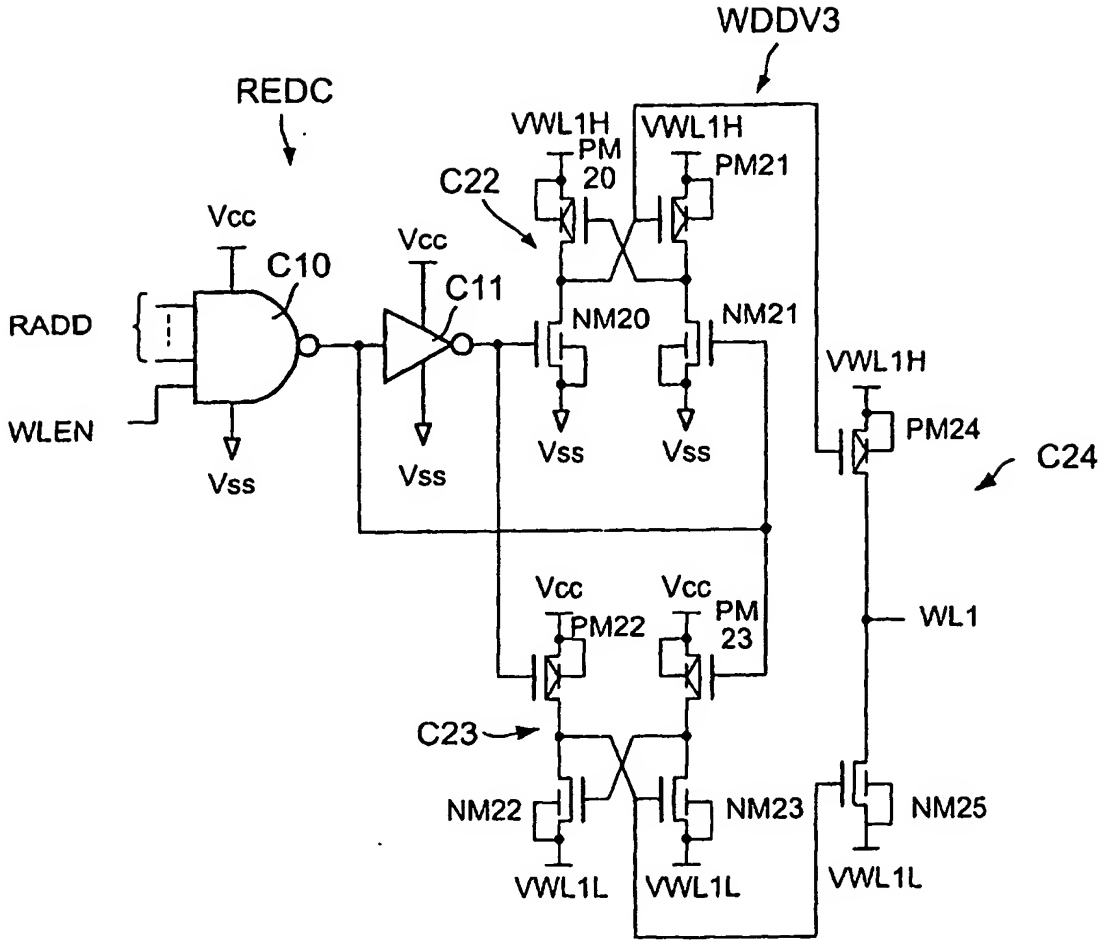
WDDV3
REDC
VWL1H
VWL1H
PM 20
PM21
C22
Vcc
Vcc
C10
C11
RADD
NM20
NM21
VWL1H
WLEN
PM24
C24
Vss
Vss
Vss
Vss
Vcc
Vcc
PM22
PM 23
WL1
C23
NM22
NM23
NM25
VWL1L
VWL1L
VWL1L

FIG. 7M

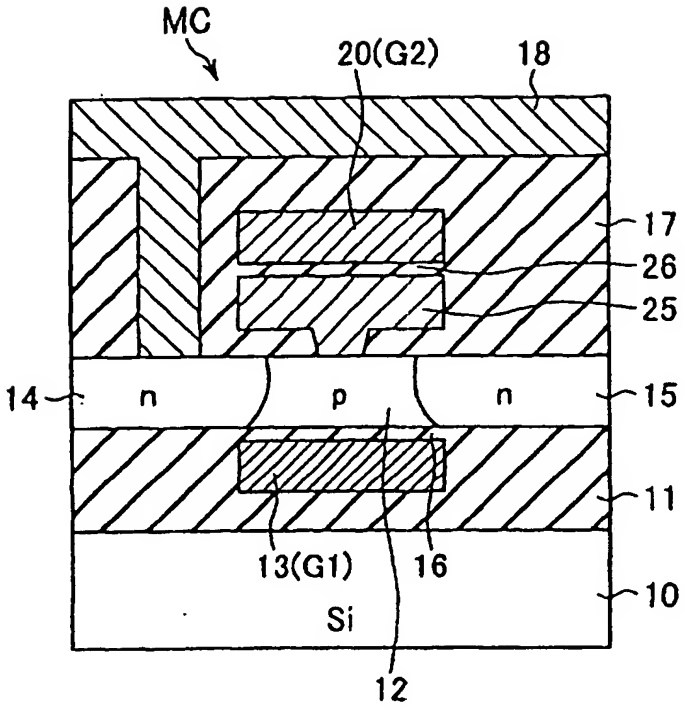

FIG. 8

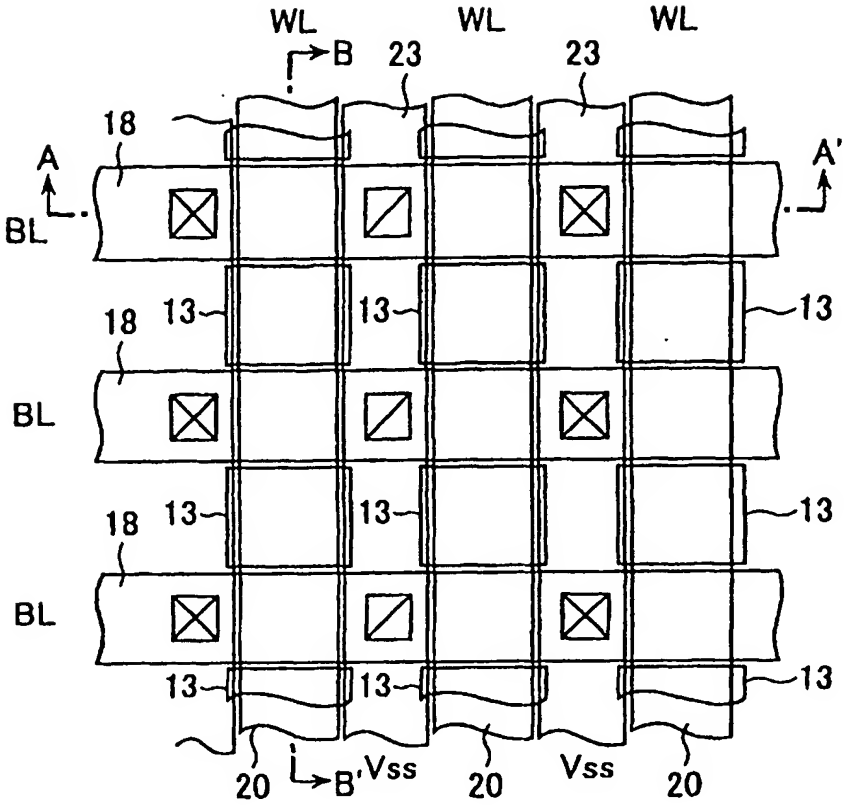
WL
WL
WL
B
23
23
18
A
A'
BL
13
13
13
18
BL
13
13
13
18
BL
13
13
13
20
B'
Vss
20
Vss
20

FIG. 10A

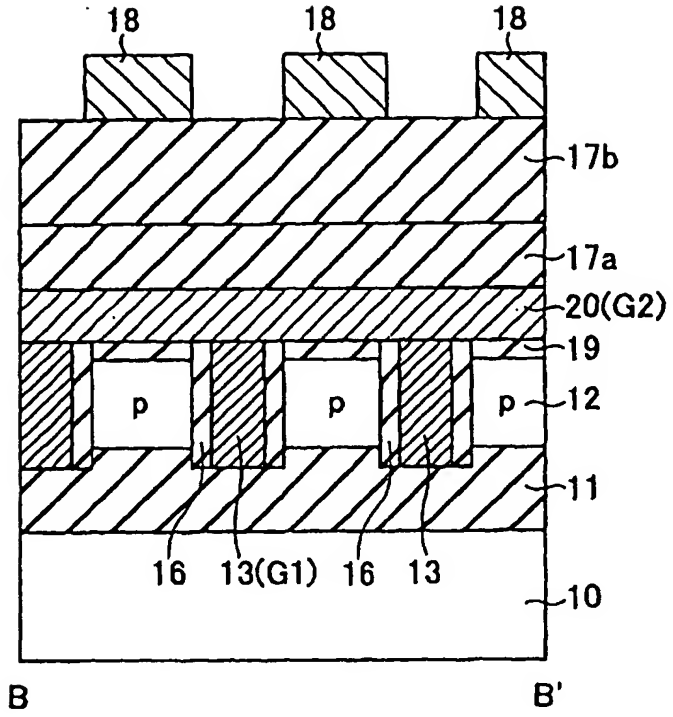

FIG. 10C

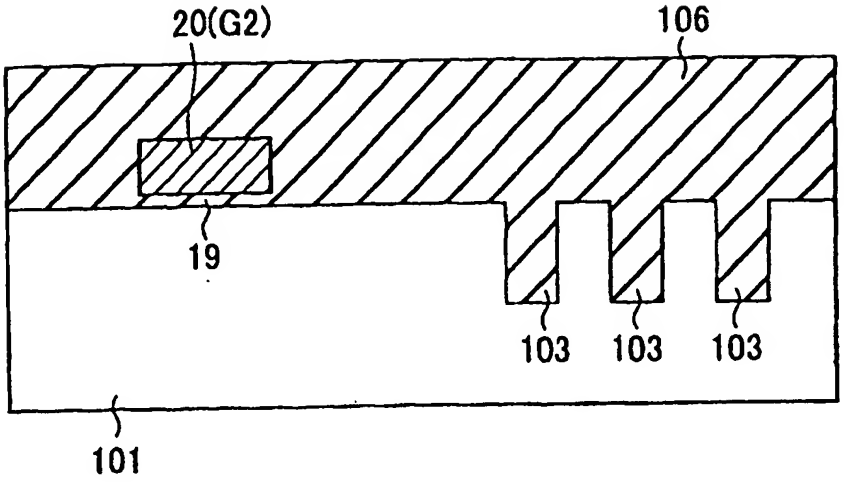

FIG. 14

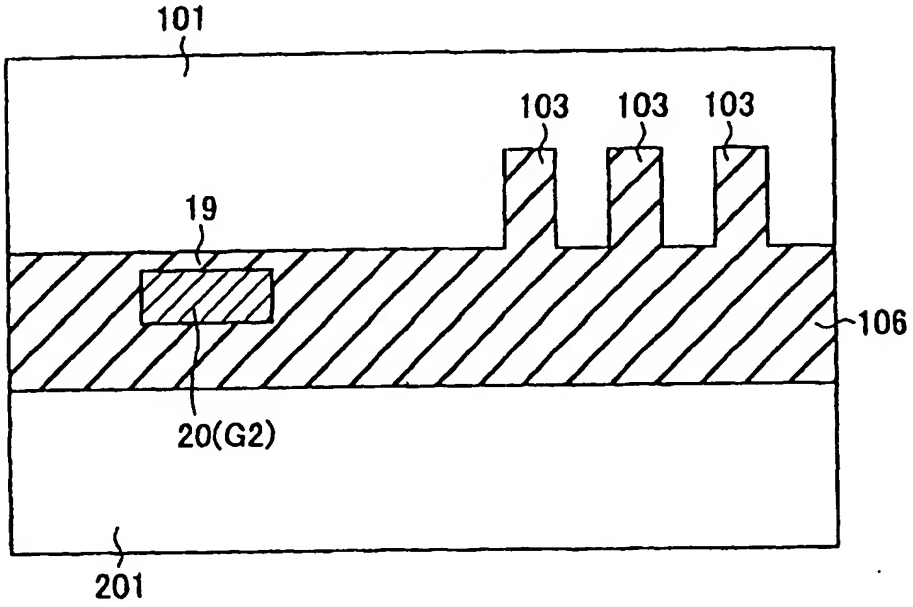

FIG. 15

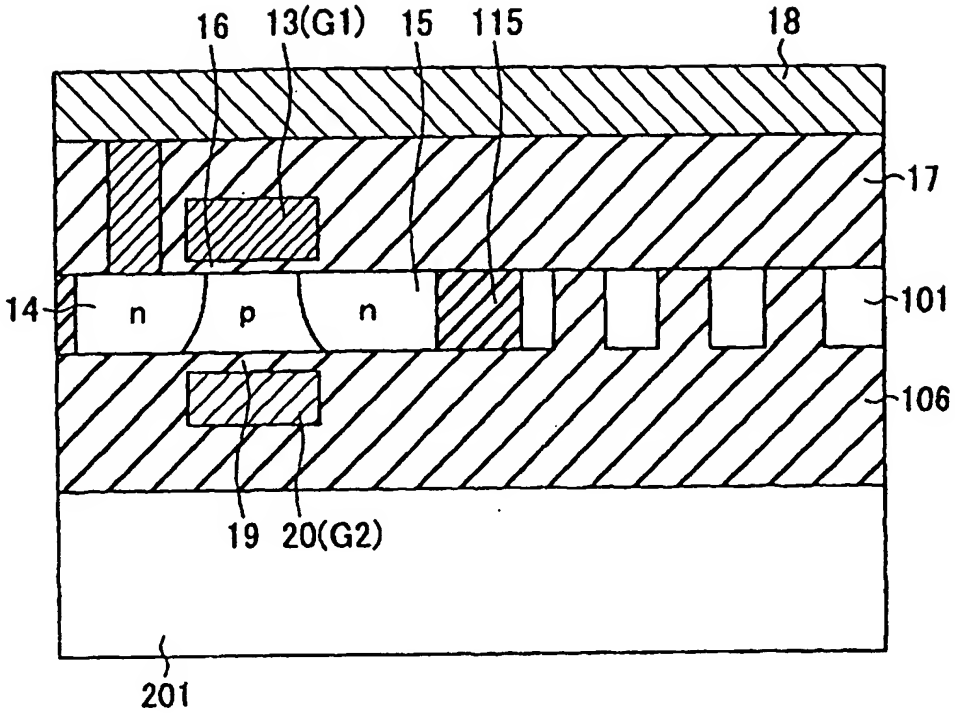
16
13(G1)
15
115
18
17
14
n
p
n
101
106
19
20(G2)
201

FIG. 18

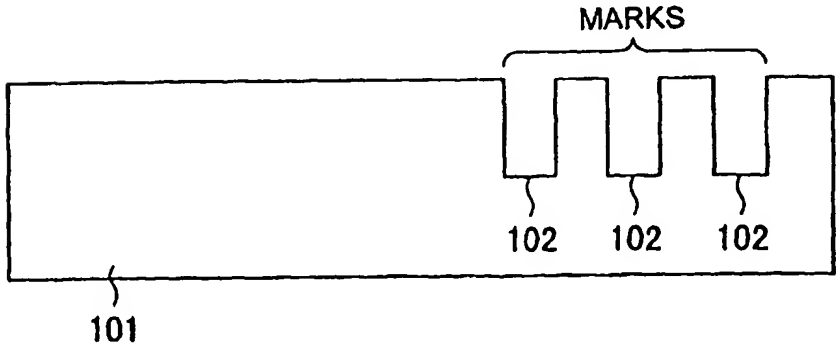
MARKS
102
102
102
101

FIG. 19

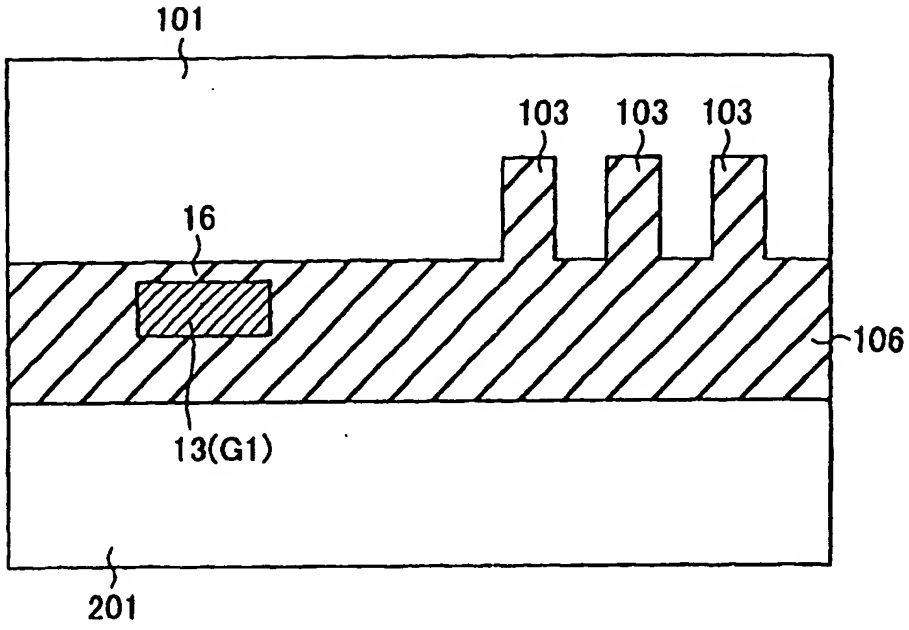

FIG. 22

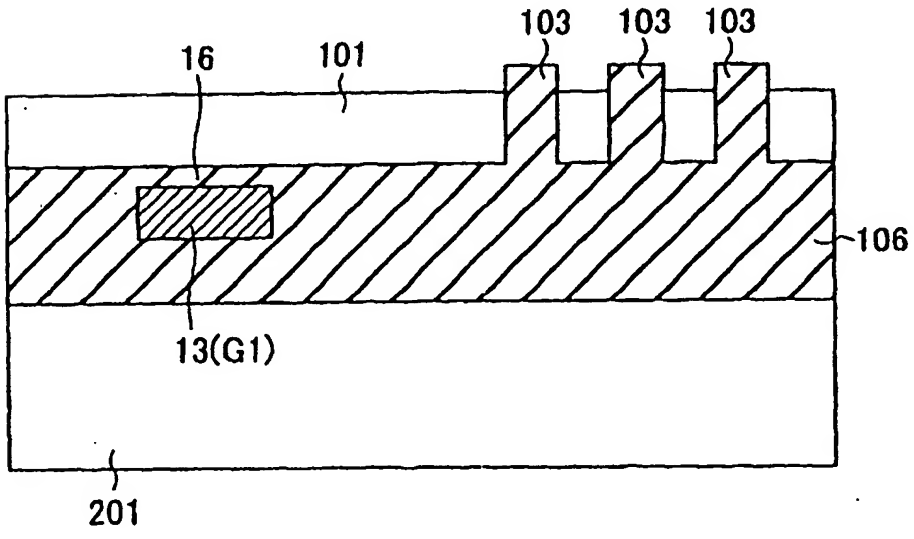

FIG. 23

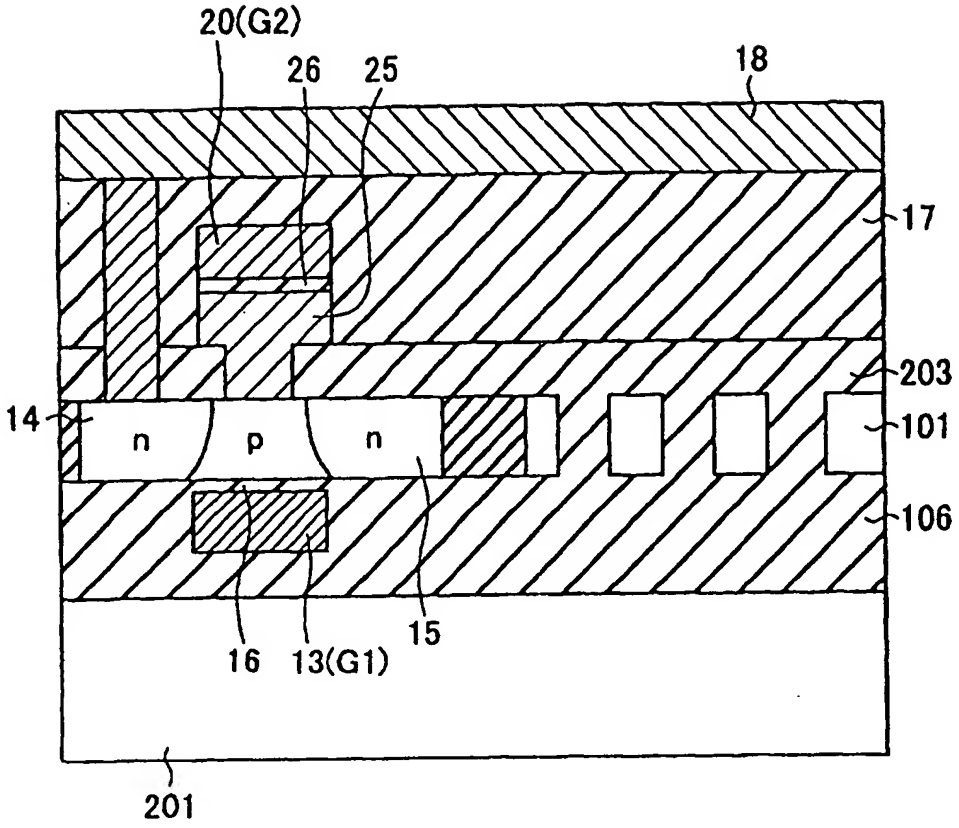
20(G2)
26
25
18
17
203
14
n
p
n
101
106
16
13(G1)
15
201

FIG. 26

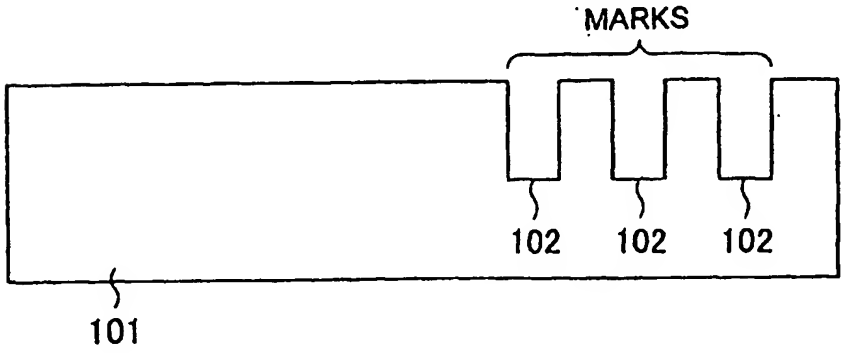
MARKS
102
102
102
101

FIG. 27

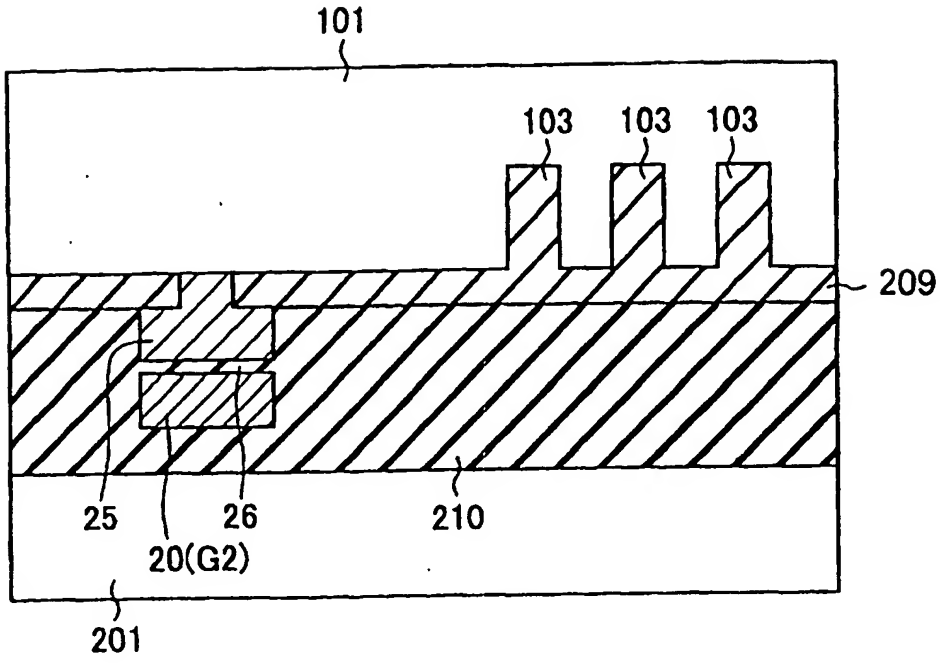
101
103
103
103
209
25
26
210
20(G2)
201

FIG. 30

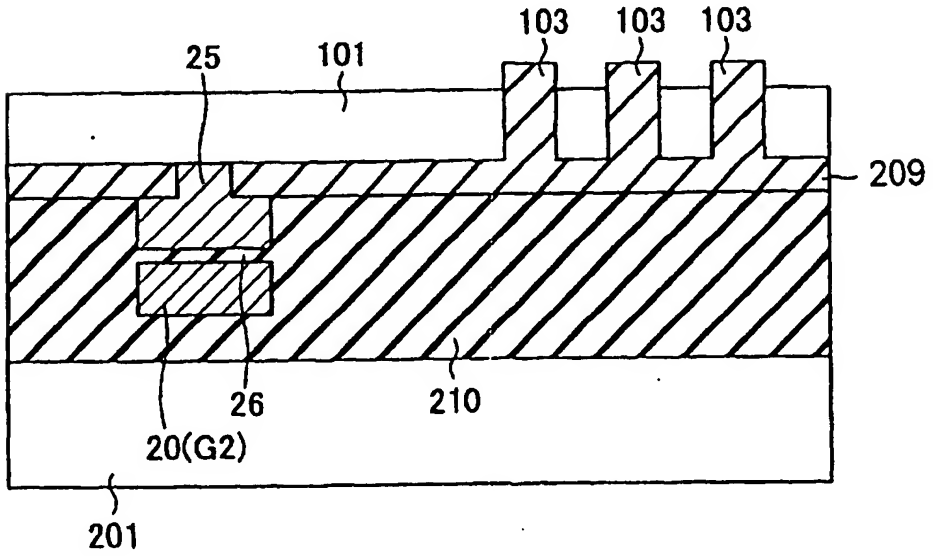
103
103
103
25
101
209
26
210
20(G2)
201

FIG. 31

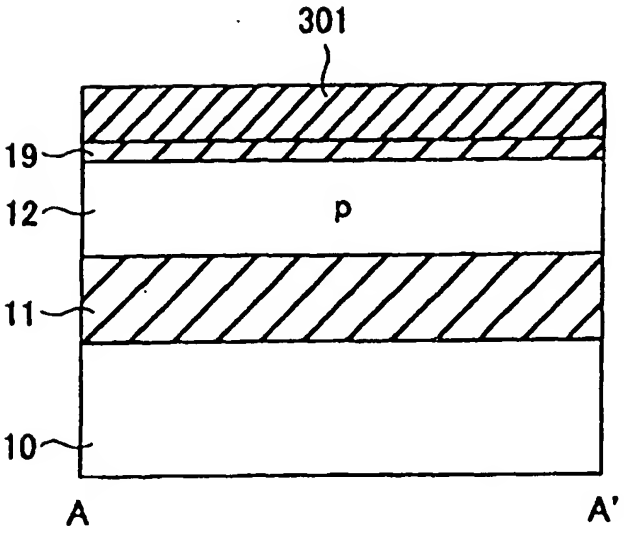

FIG. 34A

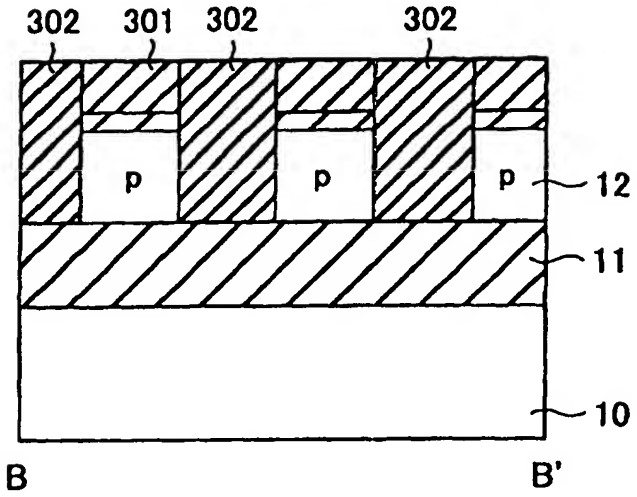

FIG. 34B

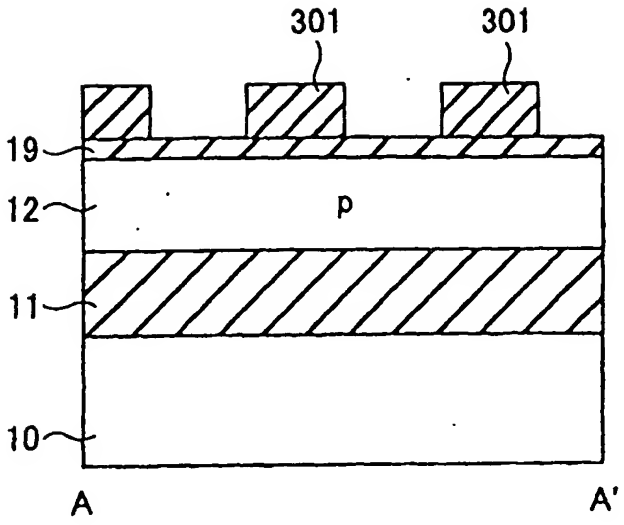

FIG. 36A

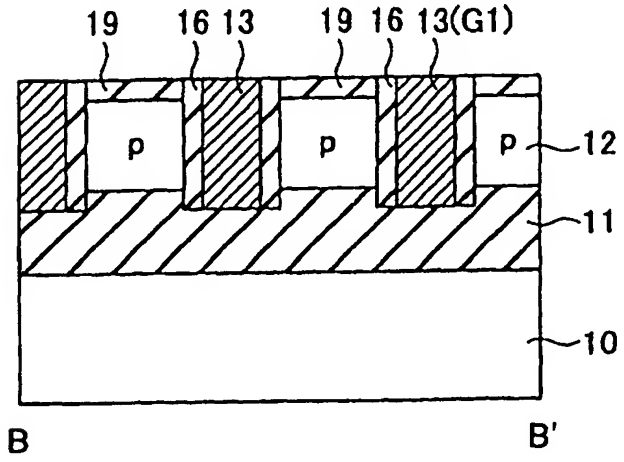

FIG. 36B

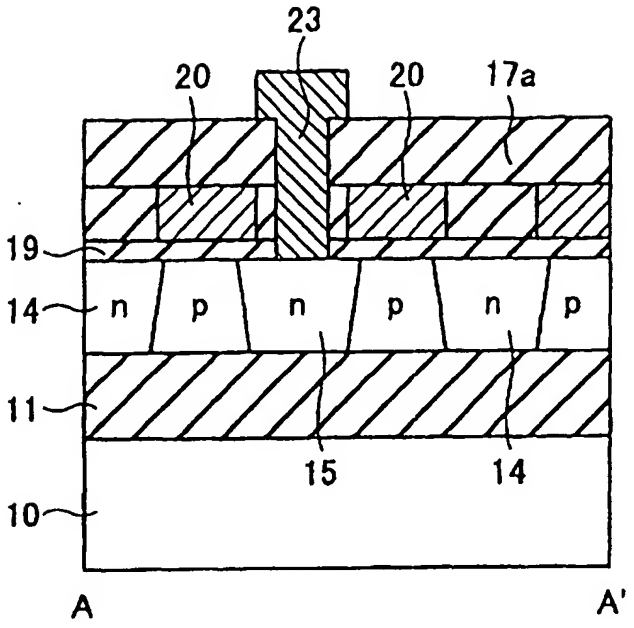

FIG. 38A

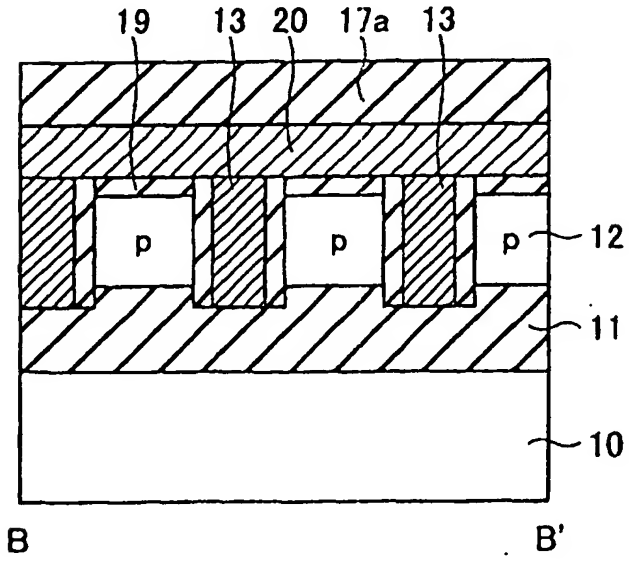

FIG. 38B

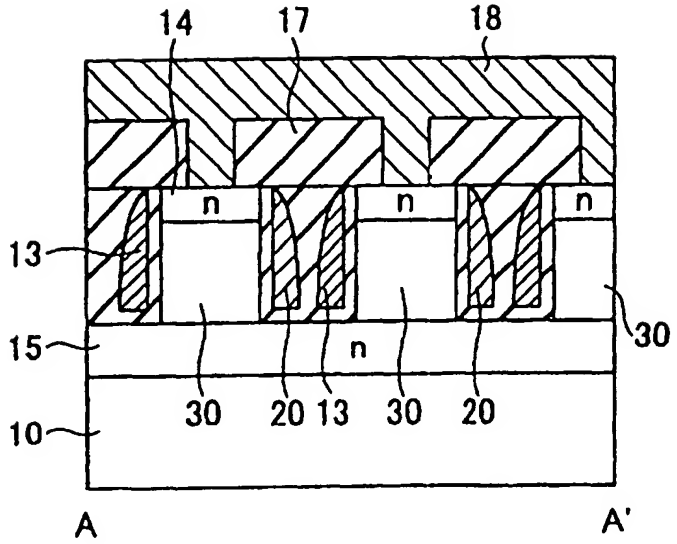

FIG. 39B

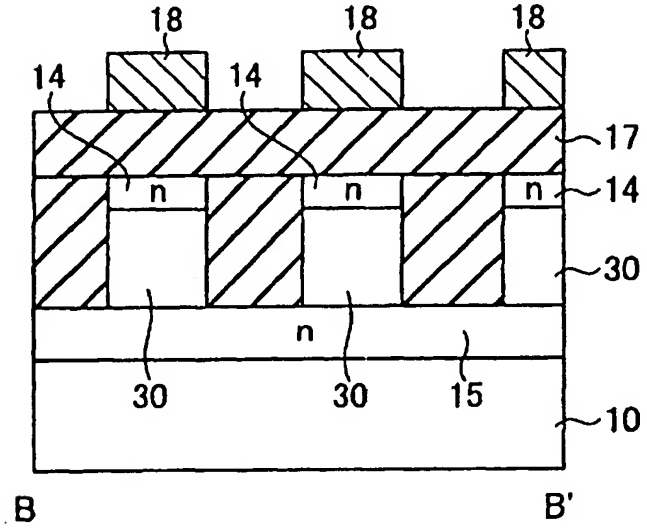

FIG. 39C

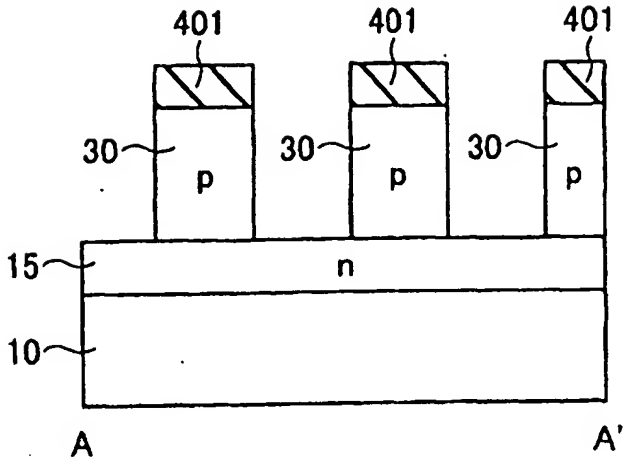

FIG. 41A

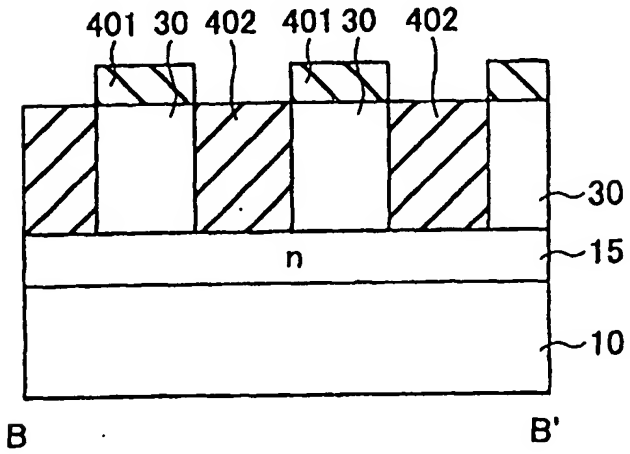

FIG. 41B

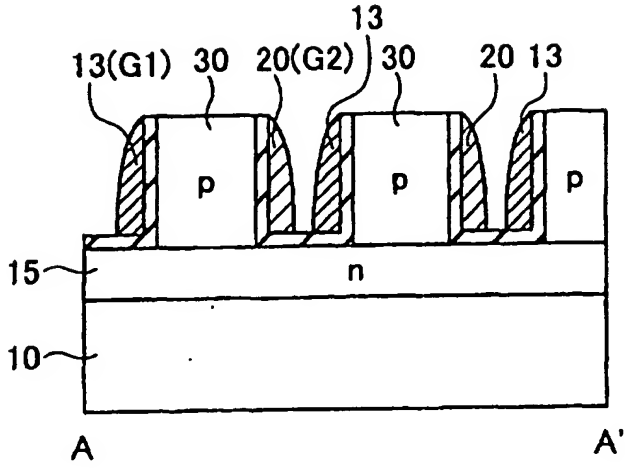

FIG. 43A

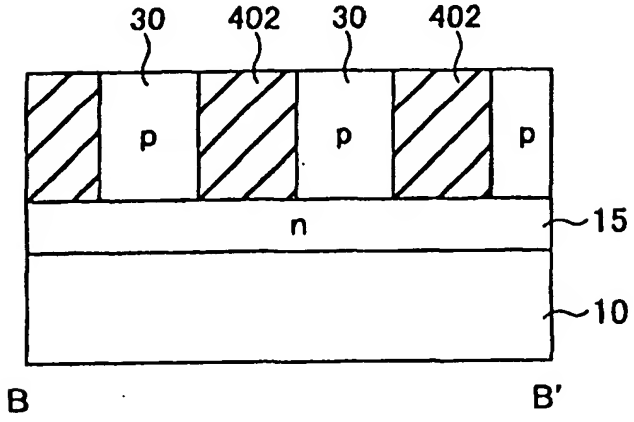

FIG. 43B

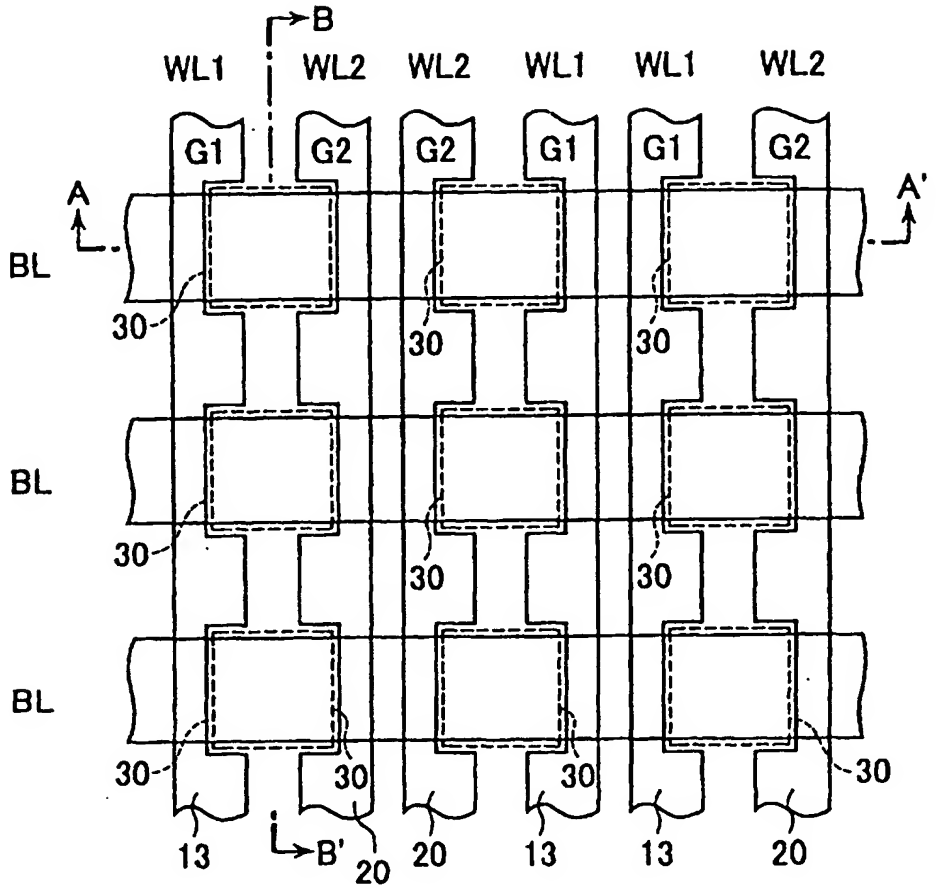
B
WL1
WL2
WL2
WL1
WL1
WL2
G1
G2
G2
G1
G1
G2
A
A'
BL
BL
BL
30
30
30
30
30
30
30
30
30
30
30
13
B'
20
20
13
13
20

FIG. 45A

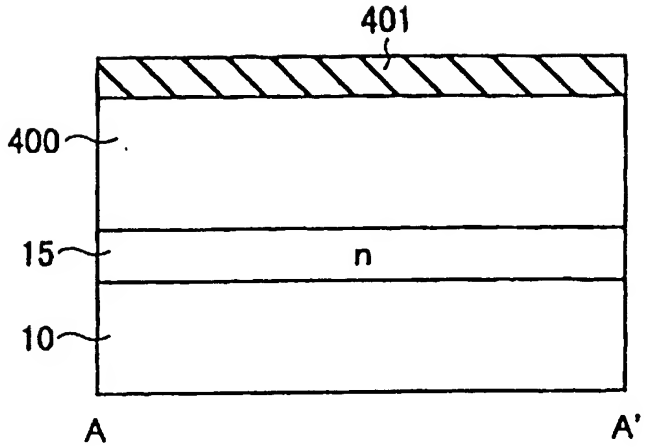

FIG. 46A

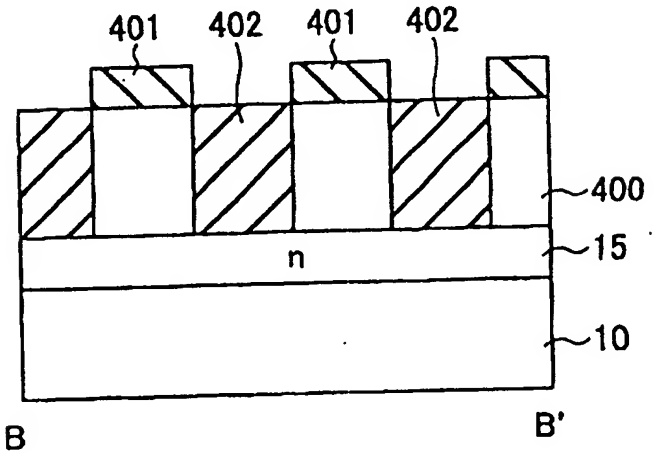

FIG. 46B

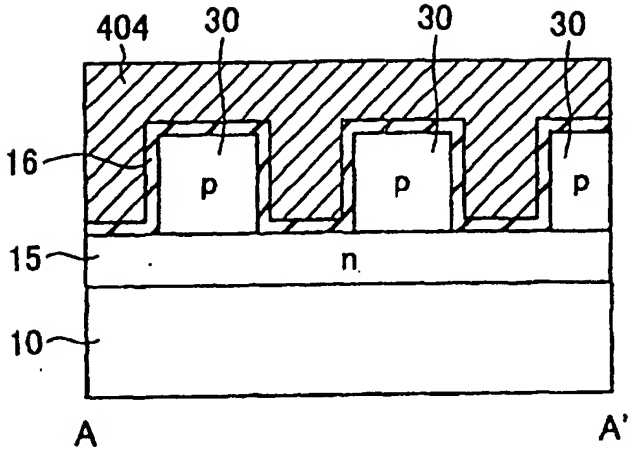

FIG. 48A

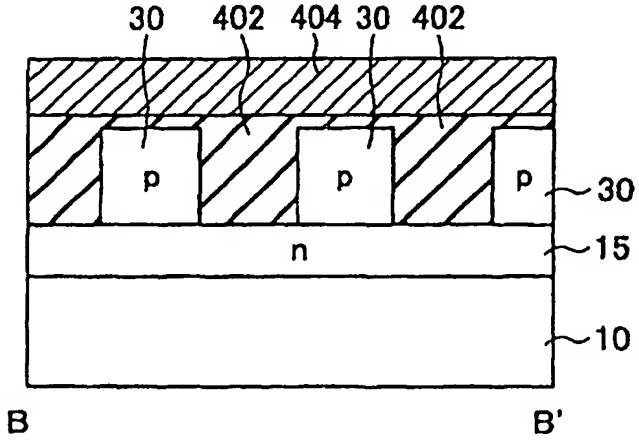

FIG. 48B

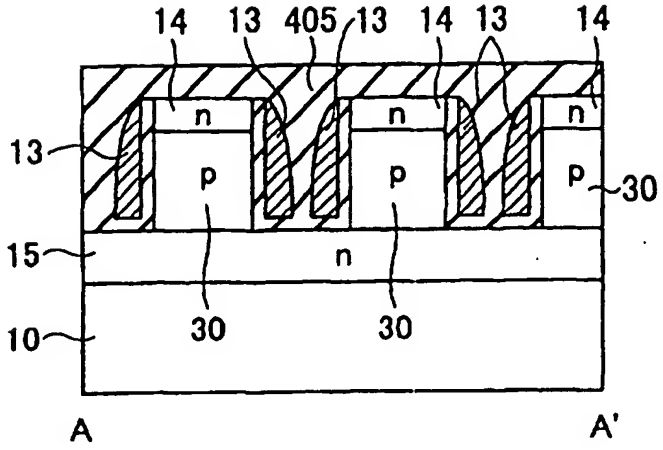

FIG. 50A

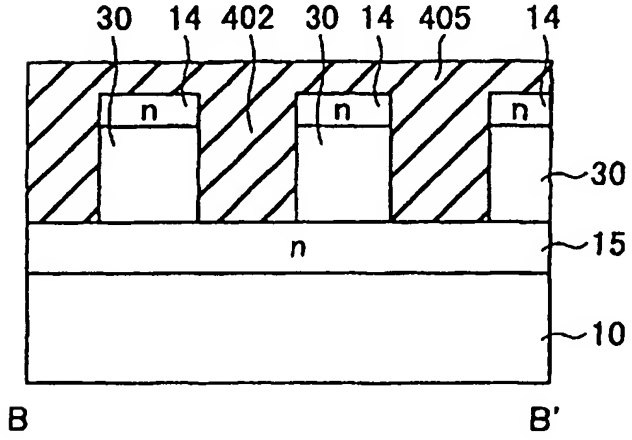

FIG. 50B

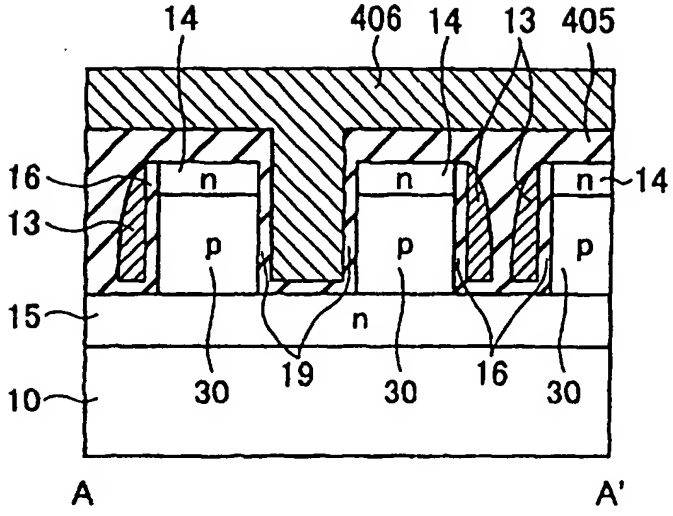

FIG. 52A

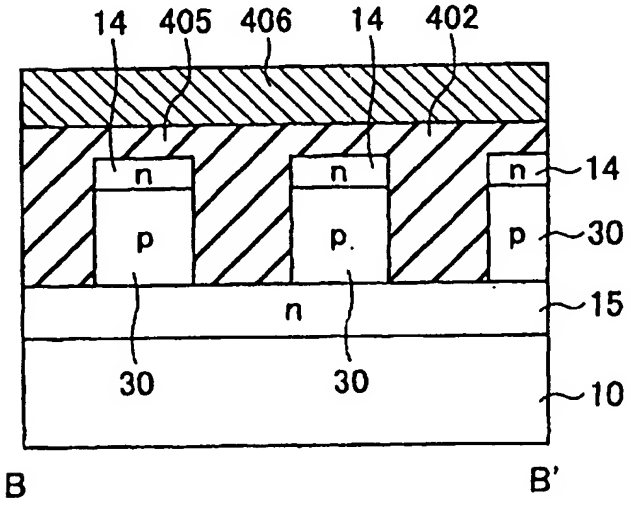

FIG. 52B

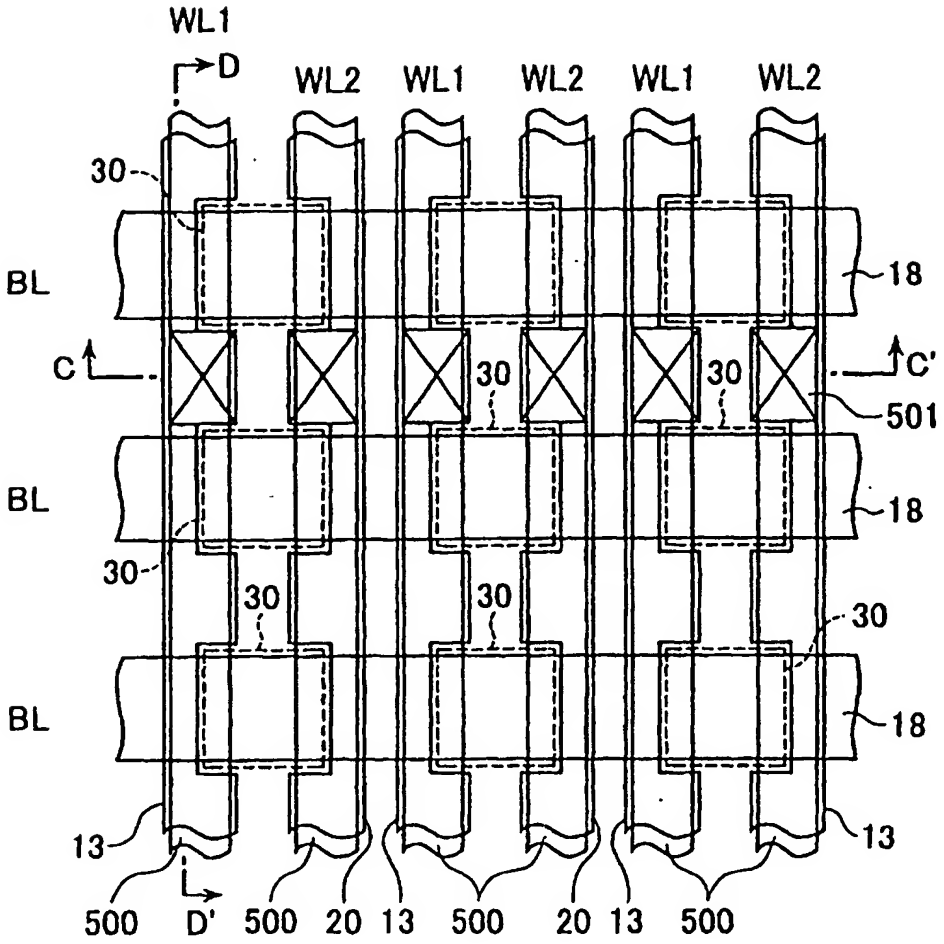
WL1
D
WL2
WL1
WL2
WL1
WL2
30
BL
18
C
C'
30
30
501
BL
18
30
30
30
30
BL
18
13
13
500
D'
500
20
13
500
20
13
500

FIG. 54A

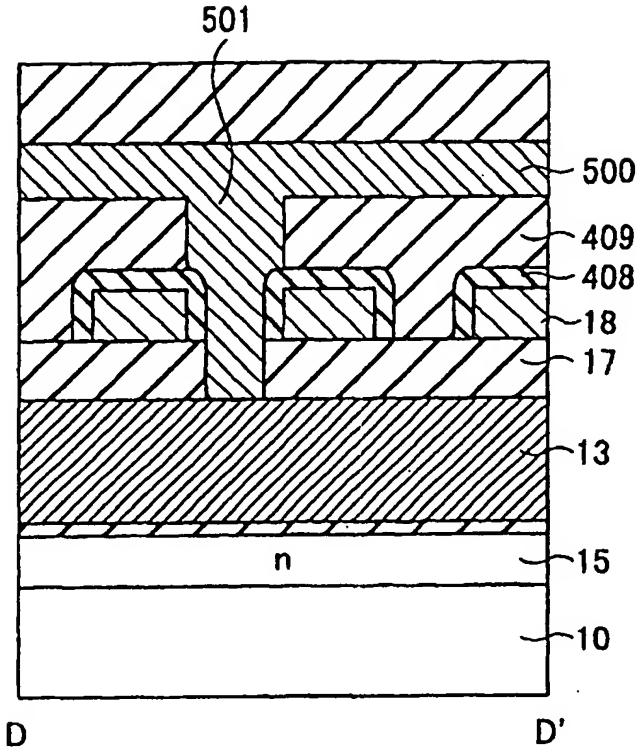

FIG. 54C

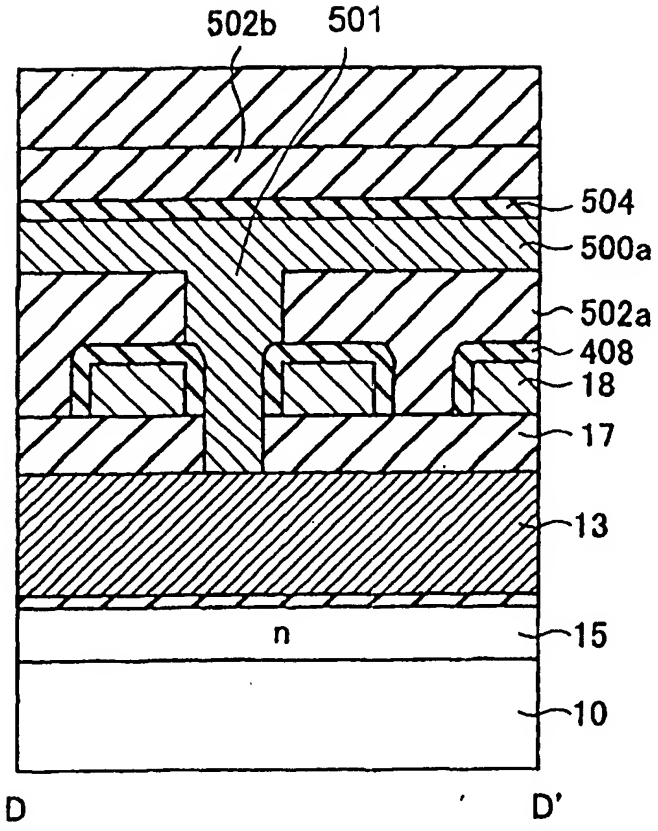

FIG. 55B

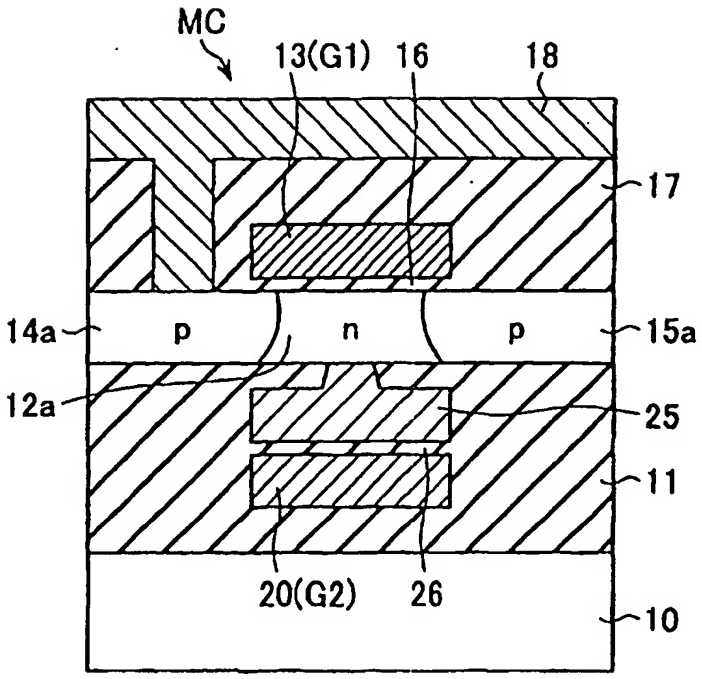

FIG. 58

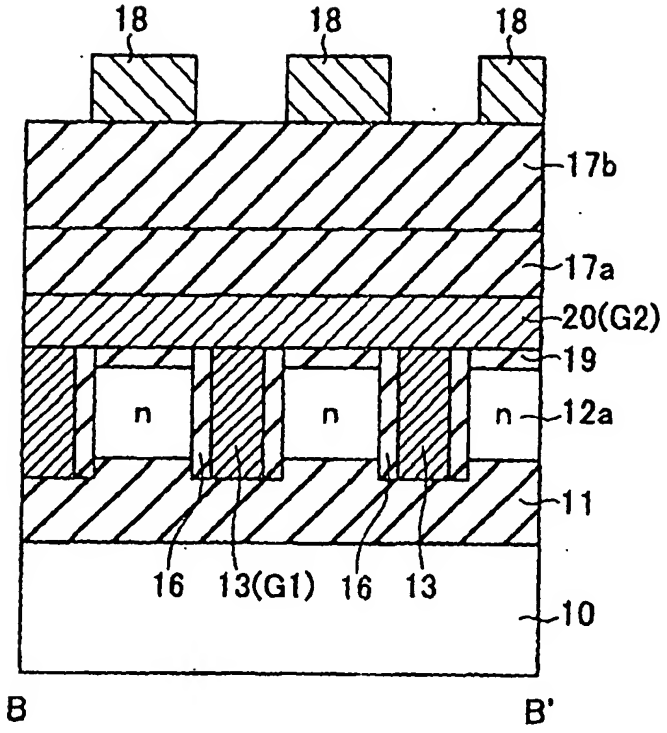

FIG. 59B

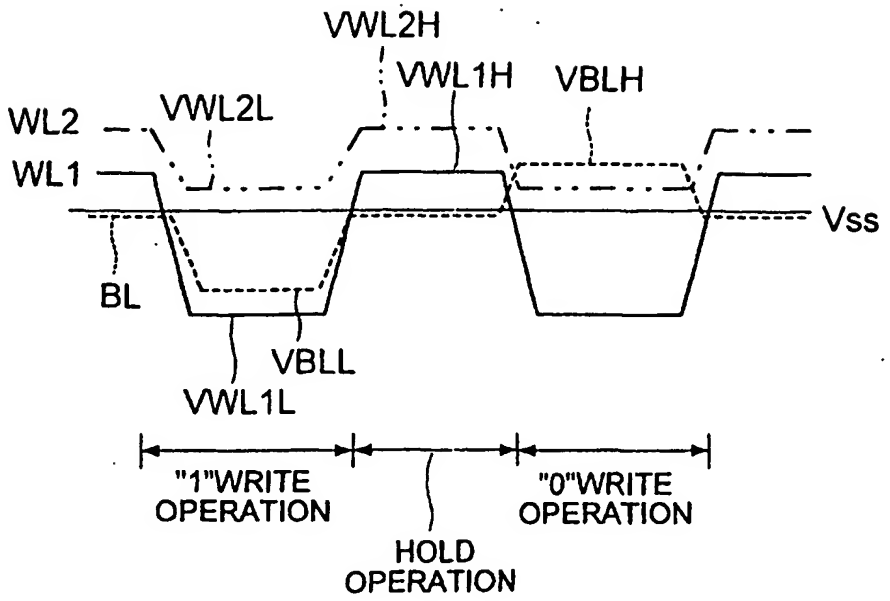

FIG. 60B

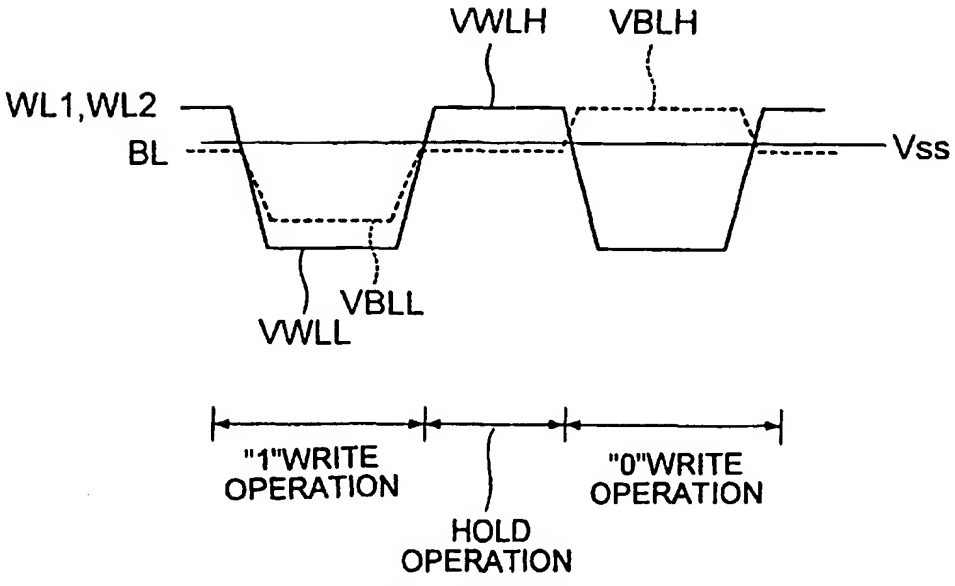

FIG. 60C

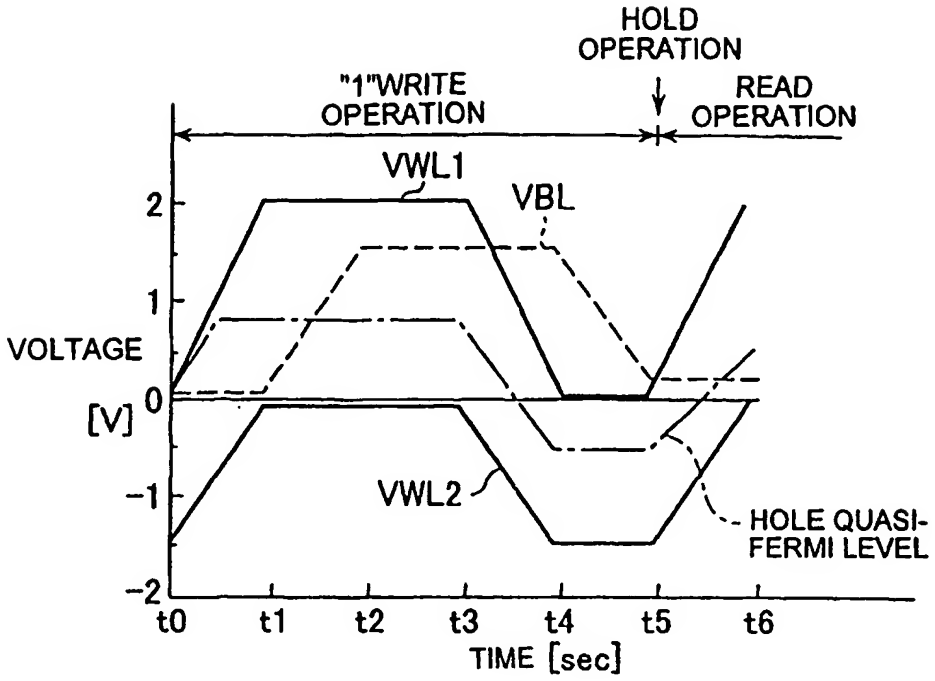
HOLD
OPERATION
"1"WRITE
OPERATION
READ
OPERATION
VWL1
VBL
VOLTAGE
[V]
2
1
0
-1
-2
VWL2
HOLE QUASI-
FERMI LEVEL
t0
t1
t2
t3
t4
t5
t6
TIME [sec]

FIG. 63

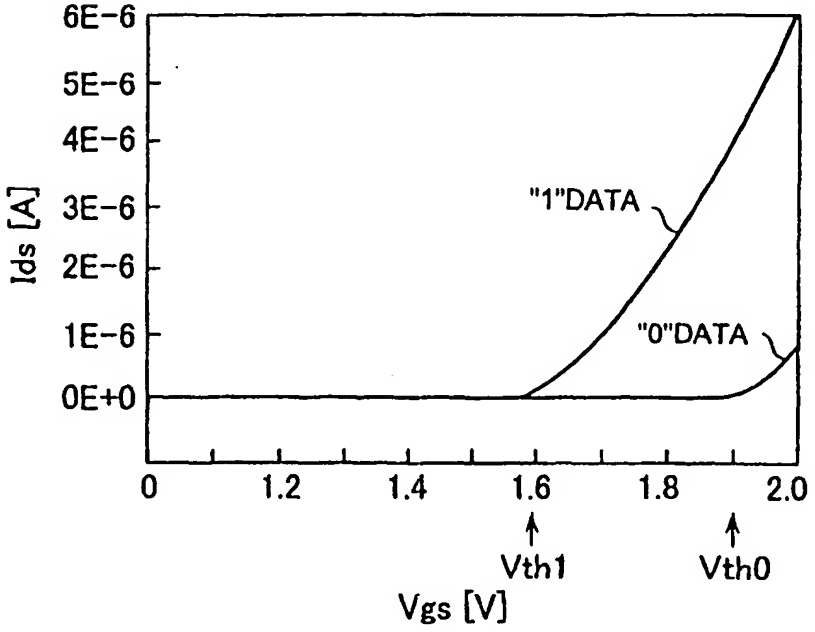
6E-6
5E-6
4E-6
3E-6
2E-6
1E-6
0E+0
Ids [A]
"1"DATA
"0"DATA
0
1.2
1.4
1.6
1.8
2.0
Vth1
Vth0
Vgs [V]

FIG. 64

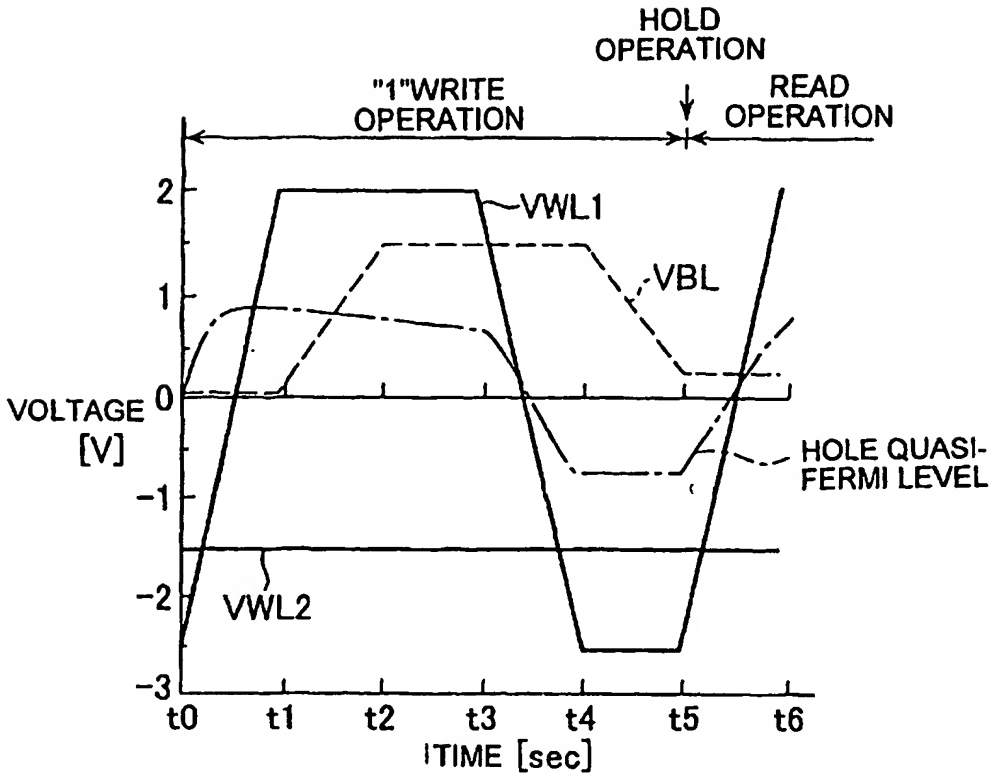
HOLD
OPERATION
"1"WRITE
OPERATION
READ
OPERATION
VWL1
VBL
HOLE QUASI-
FERMI LEVEL
VWL2
VOLTAGE
[V]
2
1
0
-1
-2
-3
t0
t1
t2
t3
t4
t5
t6
TIME [sec]

FIG. 66

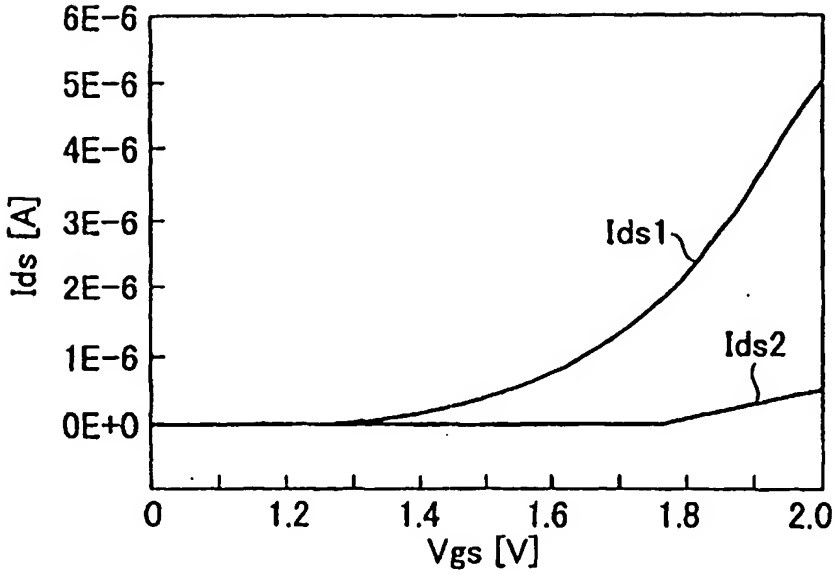
6E-6
5E-6
4E-6
3E-6
2E-6
1E-6
0E+0
Ids [A]
Ids1
Ids2
0
1.2
1.4
1.6
1.8
2.0
Vgs [V]

FIG. 67

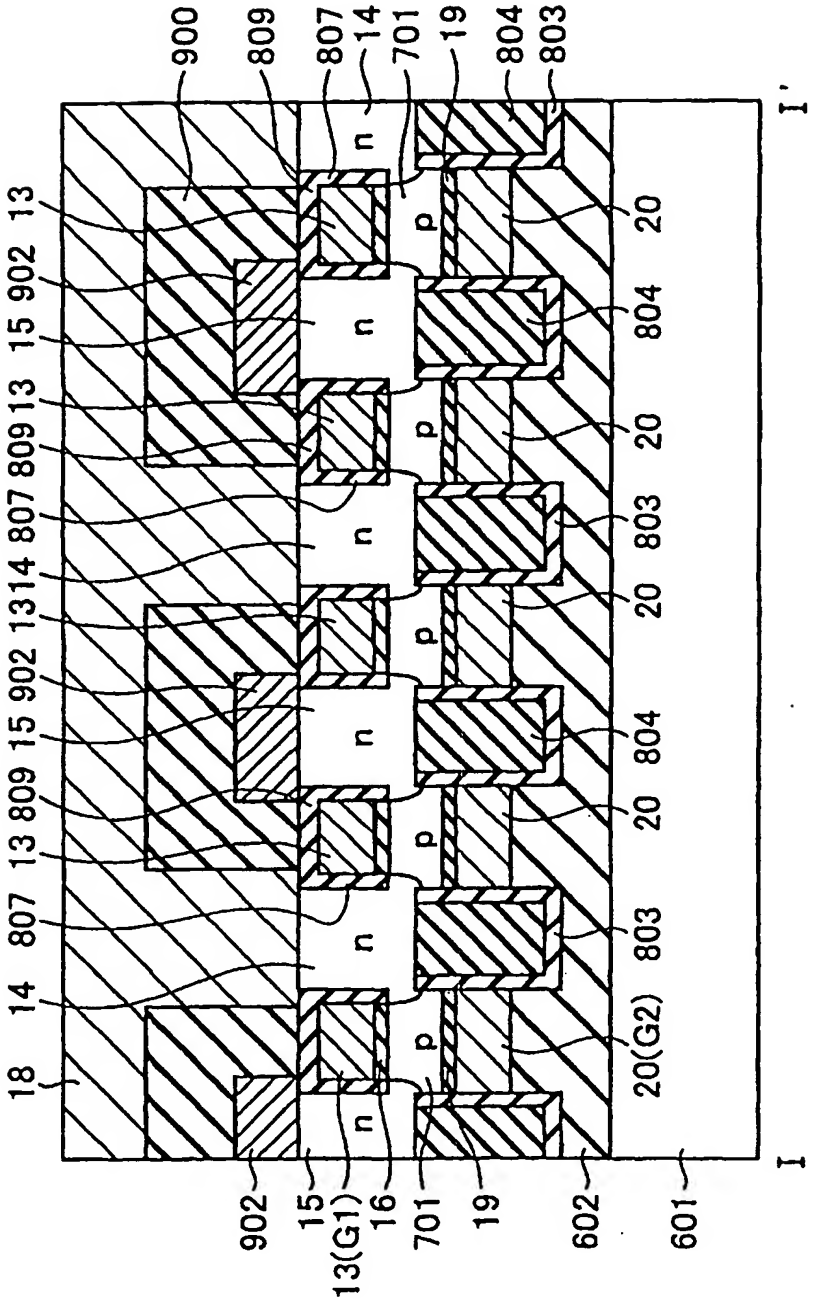
900
809
807
14
701
19
804
803
I'
13
902
15
13
809
807
13
14
902
15
809
13
807
18
14
n
p
20
804
20
803
20
804
20
803
20(G2)
902
15
13(G1)
16
701
19
602
601
I

FIG. 68B

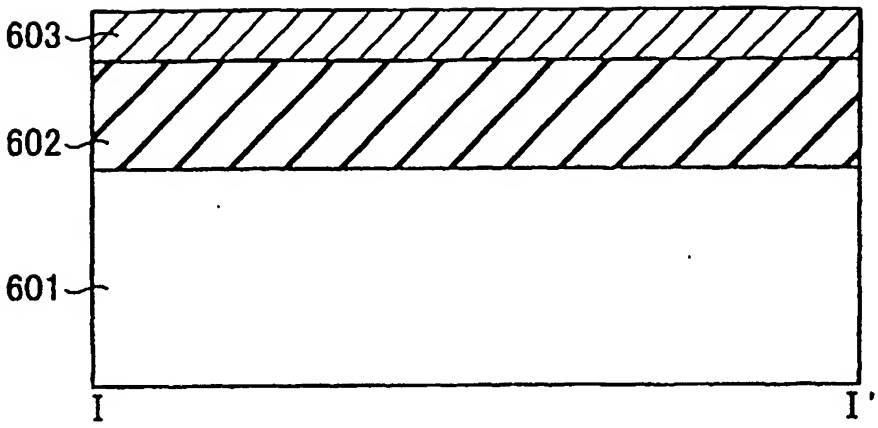

FIG. 69

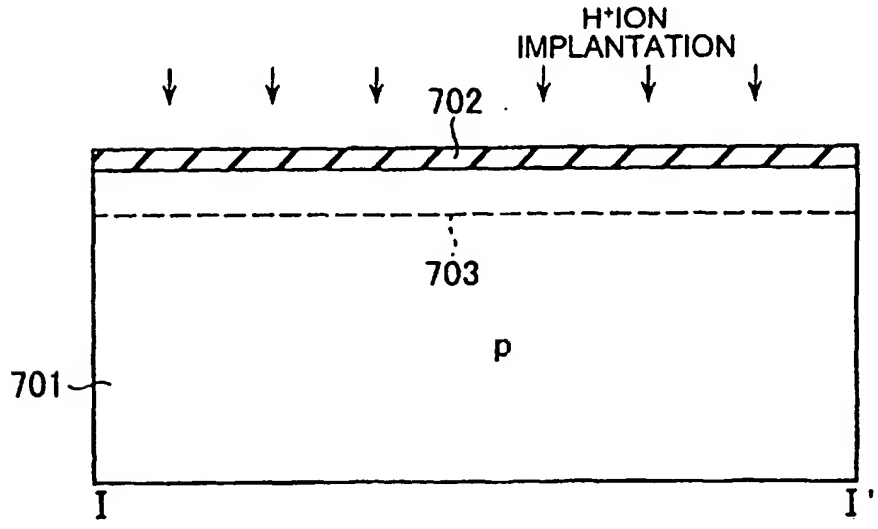

FIG. 70

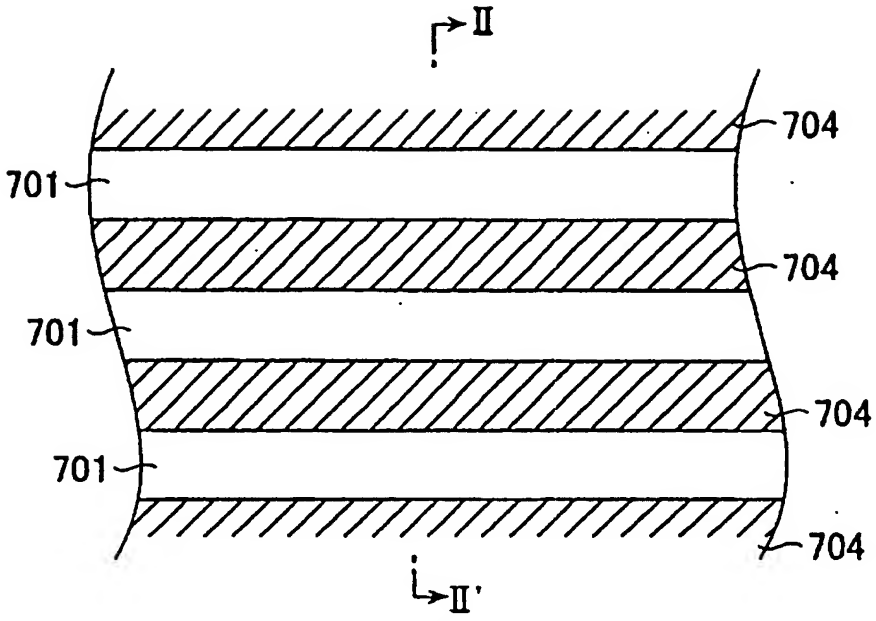

FIG. 73A

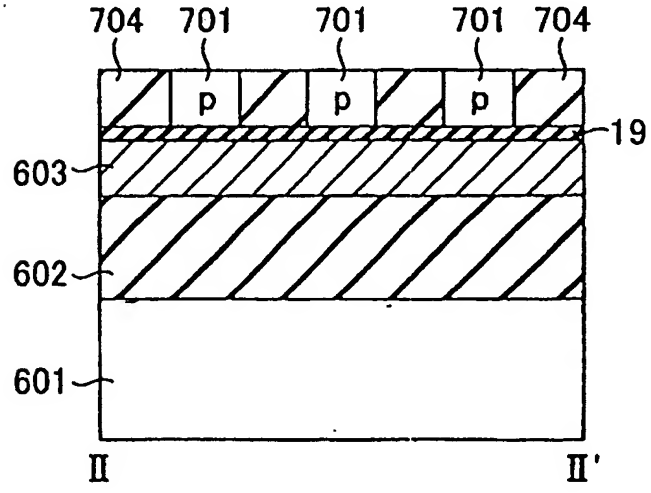

FIG. 73B

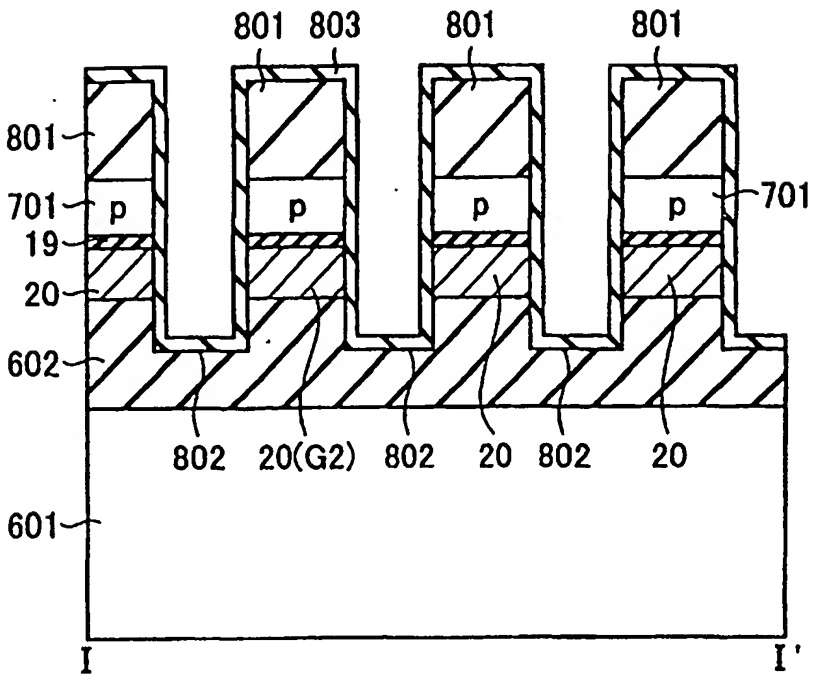
801
803
801
801
801
701
p
p
p
p
701
19
20
602
802
20(G2)
802
20
802
20
601
I
I'

FIG. 76

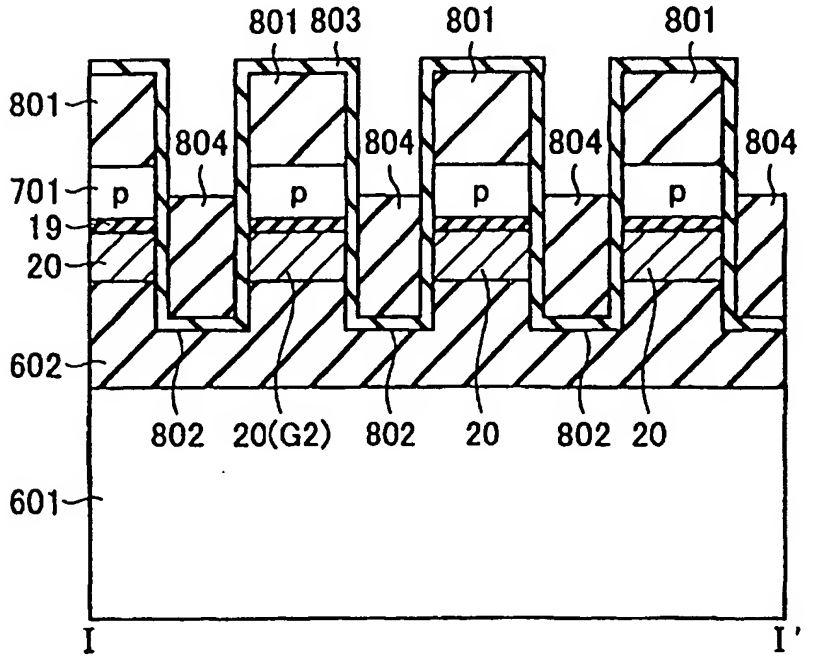
801
803
801
801
801
804
804
804
804
701
p
p
p
p
19
20
602
802
20(G2)
802
20
802
20
601
I
I'

FIG. 77

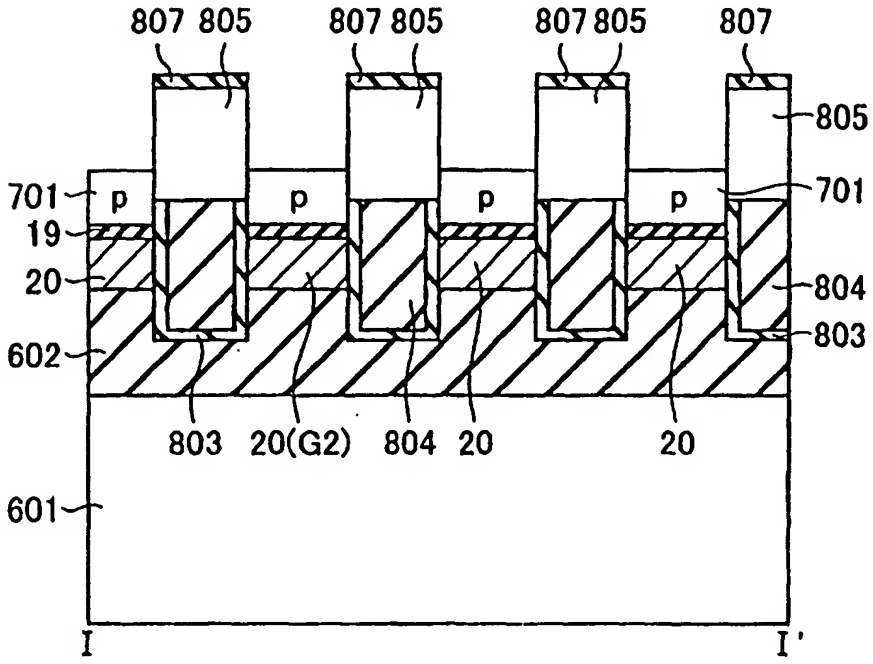
807 805
807 805
807 805
807
805
701
p
p
p
p
701
19
20
804
803
602
803
20(G2)
804
20
20
601
I
I'

FIG. 80

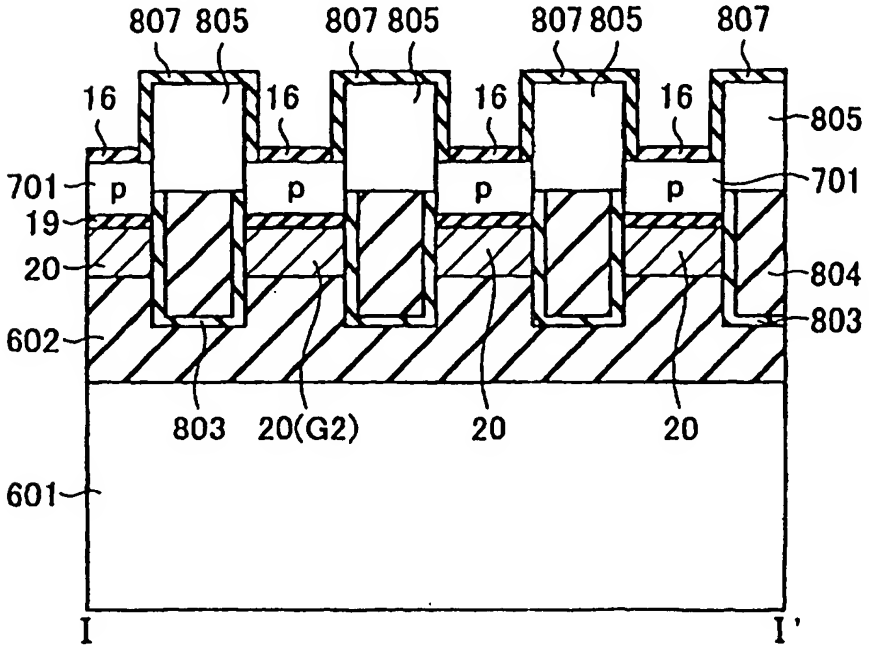
807 805
807 805
807 805
807
16
16
16
16
805
701
p
p
p
p
701
19
20
804
803
602
803
20(G2)
20
20
601
I
I'

FIG. 81

FIG. 84A

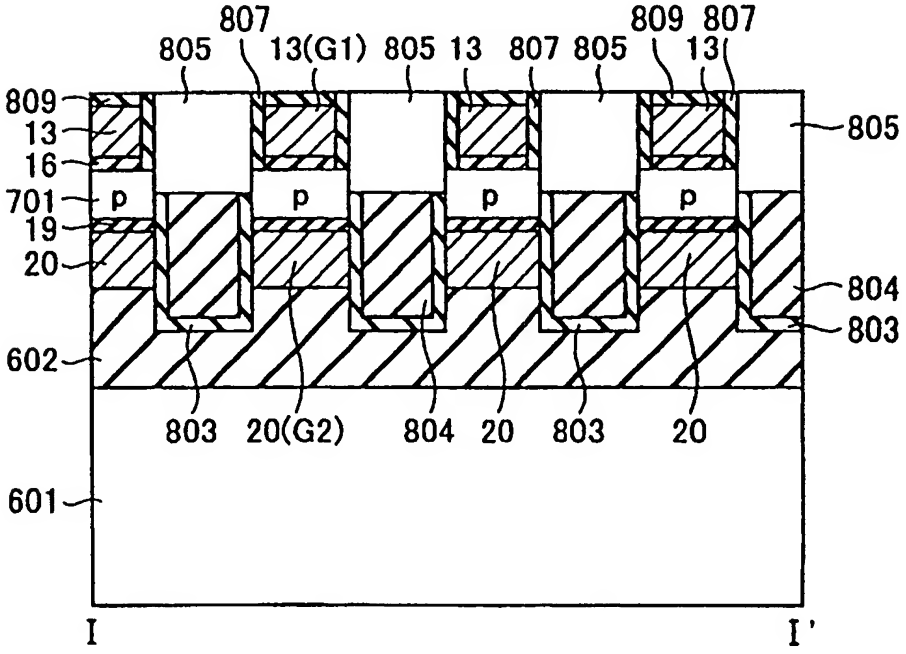

FIG. 84B

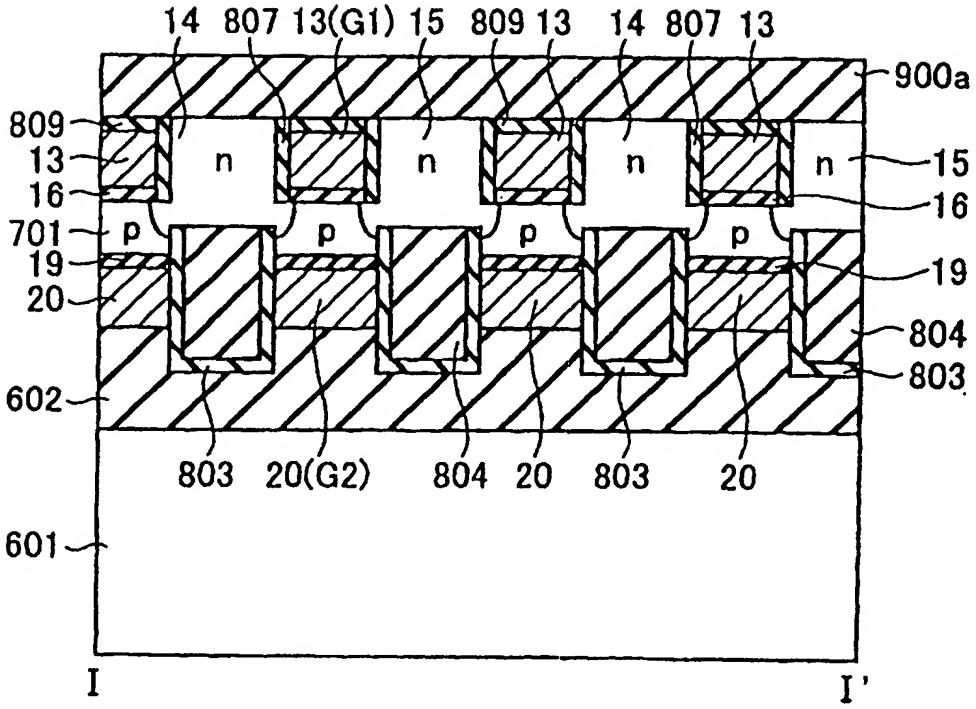
14
807
13(G1)
15
809
13
14
807
13
900a
809
13
16
701
19
20
n
n
n
n
p
p
p
p
15
16
19
804
803
602
803
20(G2)
804
20
803
20
601
I
I'

FIG. 87

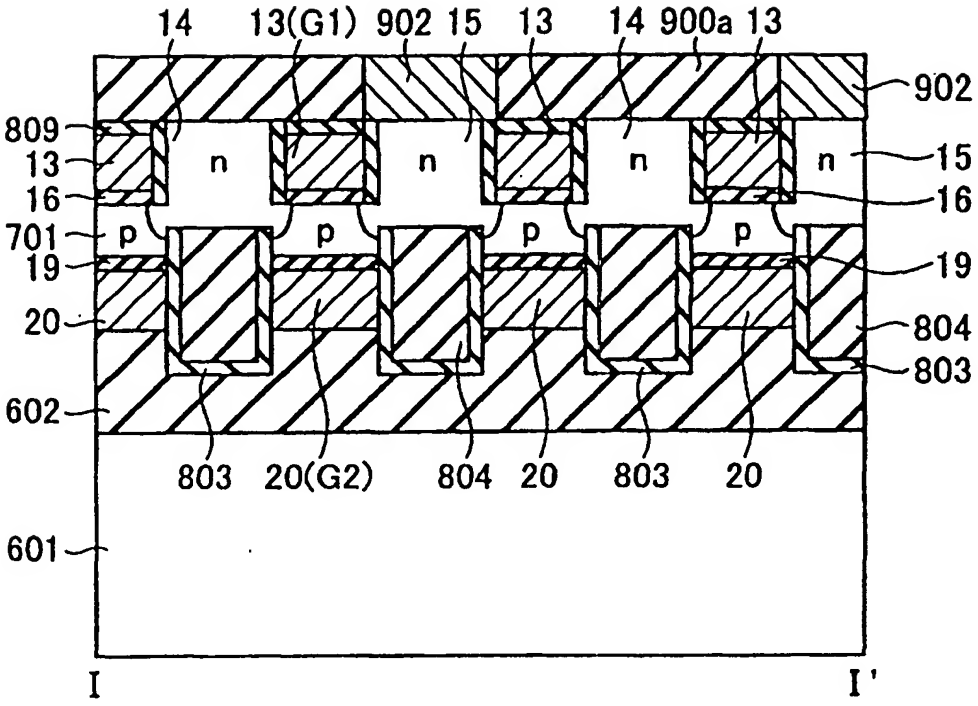
14
13(G1)
902
15
13
14
900a
13
902
809
13
16
701
19
20
602
601
n
p
15
16
19
804
803
803
20(G2)
804
20
803
20
I
I'

FIG. 89

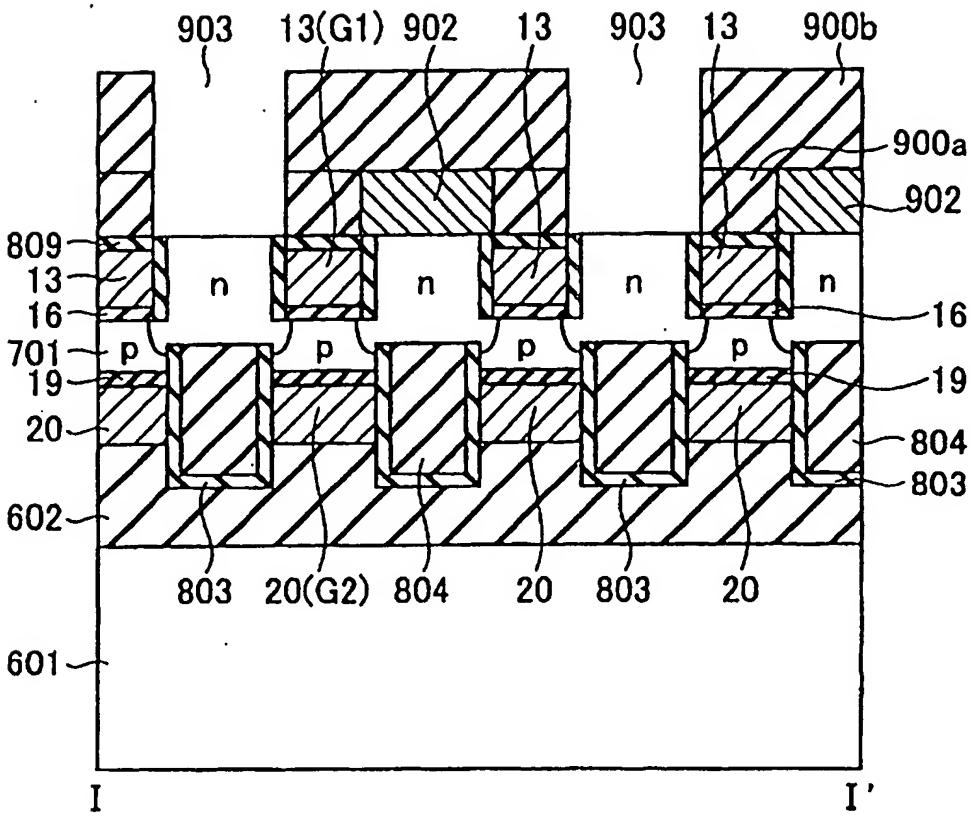
903
13(G1)
902
13
903
13
900b
900a
902
809
13
16
701
19
20
602
601
n
n
n
n
16
p
p
p
p
19
804
803
803
20(G2)
804
20
803
20
I
I'

FIG. 91